Analysis and modeling of mismatch phenomena for advanced MOSFETs

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Analysis and modeling of mismatch phenomena for advanced MOSFET

Université Joseph Fourier / Université Pierre Mendès France / Université Stendhal / Université de Savoie / Grenoble INP

To My Mum and the Memory of my dad

You are always present in my heart, in my mind and in every step of my life..

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List of acronyms

MOSFET: Metal-Oxide-Semiconductor Field Effect Transistors

SRAM: Static Random Access Memory

EOT: Electrical Oxide Thickness

SCZ: Space Charged Zones

FD SOI: Fully Depleted Silicon On Insulator

PD SOI: Partially Depleted Silicon On Insulator

BOX: Buried Oxide

SCE: Short Channel Effect

DIBL: Drain Induced Barrier Lowering

RDF: Random Dopant Fluctuations

LER: Line Edge Roughness

PGG: Poly-Gate Granularity

MGG: Metal Gate Granularity

LDE: Lateral drain extended

NBTI: Negative-Bias Temperature Instability

General Introduction

General challenges in Microelectronics

As its name suggests, the field of microelectronics focuses on the study and fabrication of electronic components at the micro and nano scale, connected together on the same substrate to form Integrated Circuits (IC). The role of IC is to implement one or many electronic functions of different complexity levels on the same chip. IC find extensive use in electronic systems such as smart phones, numerical televisions, credit cards, computers, videogame consoles, devices for automotive, military and even aerospace applications. Any perspective progress towards enhancing such systems starts from improvements in the field of microelectronics. The driving parameters in research aimed at achieving enhanced IC performance are speed, integration density, and reduced power consumption and production costs.

The basic components of integrated circuits are transistors, diodes, resistors, capacitors, and inductors. In 1965 Gordon Moore in [Moore 65] predicted that the number of transistors that can be hosted in circuits of a given size will roughly double with every year of development, enabling exponential improvement in system-level performance. Moore revised his prediction at a later date [Moore 75] and modified it by stating that the number of transistors in microprocessors would double every two years. This prediction is known as "scaling trend", and reflects the research efforts that pursue the continuous miniaturization of the dimensions of MOS transistors. MOS with reduced size achieve high saturation current, which translates into an increase in the operating speed of the products. The challenge with such devices is however to maintain the leakage current low enough in order to limit the power consumption of products, especially if powered by batteries.

Another challenge faced by researchers chasing the "scaling trend" is the transistor local variability. This phenomenon is a consequence of process variations (random microscopic fluctuations of the device architecture) and causes identically designed transistors to exhibit different electrical behavior. It became mandatory, therefore, for the microelectronics industry to understand the physical causes of such variability, to quantify them, and to propose

solutions that enable reduced variability, with the aim of guaranteeing reliable performance in integrated circuits.

Motivation of this work

For correct operation, certain analog (current mirrors, amplifiers, etc.) and digital (Static Random Access Memory, SRAM) circuits require pairs of transistors, which are identically designed and laid out in an identical environment, in order to ensure identical electrical performances. Real devices, however, suffer from random local variations in the electrical parameters, a problem referred to as mismatch. Pelgrom *et al*. demonstrated a mismatch law that establishes a direct dependency between the local fluctuations of an electrical parameter P and the channel area (denoted as S) through a coefficient A [Pelgrom89]. This, in combination with the miniaturisation of MOSFET devices, has set the ground for an increasing interest in achieving a deeper understanding of the causes of the mismatch phenomena and characterising their effects, with the objective of guaranteeing reliable integrated circuits performance.

In light of the presented scenario, the purpose of the work reported in this thesis is to:

- Optimize the measurement methodology of mismatch phenomena;
- Characterize different configurations of MOS transistors in order to propose optimized design architectures for specific applications;
- Analyze and model the mismatch phenomena observed in advanced Bulk and Silicon On Insulator (SOI) MOSFET transistors;
- Analyze and model the mismatch phenomena with the transistor aging in advanced MOSFET transistors.

Thesis layout

The first chapter presents the concept of MOS transistor, reviews extraction techniques and the principles of variability. The following chapters are centered on four major subjects, as outlined below.

- Chapter II focuses on the methodologies for the extraction and modeling of the electrical parameters of MOS transistors. A new methodology of mismatch extraction parameters is proposed, with a thorough discussion of its advantages and applications. A new drain current mismatch model is also proposed which expands from the strategy published by Croon [Croon07] by adding an Rsd contribution and neglecting the mutual correlation between parameters.

- Chapter III focuses on the characterization of MOS transistors of different design architectures in various configurations for high drain current design applications. A comparison of three different MOS transistor types and configurations for high drain current applications is reported. Conclusions and perspectives are discussed in detail, with the aim of proposing the most convenient MOS configuration or type for specific applications.

- After these methodology and design considerations, the studies are oriented on mismatch phenomena in advanced technologies:

    - Chapter IV treats the effect of Germanium (Ge) on mismatch phenomena in the case of the PMOS 28 nm Bulk technology node. The conducted work comprises a detailed study on threshold voltage, current gain factor and drain current for transistors with and without pocket implants.

    - In chapter V, the contribution of the metal gate granularity to electrical parameters mismatch is studied and potential solutions to eliminate the associated effects are discussed. This study is conducted on 20nm Gate–last BULK technology, and a performance comparison is presented with respect to the 28nm Bulk technology. A general review of the mismatch contributions in Bulk technology is further discussed by analyzing the observed trends over the technology nodes from 90nm BULK ST down to 20 nm.

    - Chapter VI discusses two aspects of advanced FDSOI technologies. The mismatch trends of 14nm Fully Depleted Silicon On Insulator (FD SOI) technology are first presented, followed by a comparison with the 28nm FD

SOI technology. The second aspect is instead centered on the mismatch trends observed with MOS transistor aging. To this end, NBTI stress tests have been conducted on PMOS 28nm FDSOI transistors, and a general study of the mismatch of electrical parameters as a function of the quantity of produced traps or defects is presented.

A final section concludes this manuscript by summing up the reported findings and offering perspectives for future work.

Chapter I

Transistor MOSFET: Theory, characterization and mismatch concept

After a brief description of MOS transistor concept, types, operation regimes and electrical parameters, this chapter mainly discusses the different types of electrical variability, focusing particularly on the concept of stochastic mismatch.

This chapter is divided in eight sections:

- Section I presents the concepts of Bulk MOS transistor and operation regimes.
- Section II is focused on the electrical parameters extraction methods used in this thesis.
- Section III introduces the different types of electrical variability.
- Section IV explains the local variability phenomenon called mismatch and further presents the differentiation between stochastic and systematic mismatch. This section also explains in detail the mismatch causes, extraction techniques, and effects.
- Section V describes the measurement system and the test structures used in this thesis to characterize the stochastic mismatch.
- Section VI presents the present state of the art for BULK technology in terms of mismatch.
- Section VII explains the improvement in MOS transistors performance achieved by adopting the SOI technology. This section also provides a detailed description of the state of the art for this technology in terms of mismatch.
- Finally, section VIII draws global conclusions from all the concepts illustrated in the chapter.

I.1 MOSFET transistor

One of the basic elements of integrated circuits is the Metal Oxide Semiconductor Field-Effect (MOSFET) transistor. This device is comparable to an electrical switch, as its principal function is to alternatively pass or block an electrical current. The MOS transistor in Figure I. 1 is fabricated on bulk silicon, over active zones isolated by two trenches of oxide called STI (shallow trench isolation). It is mainly composed of:

- A silicon substrate doped P (NMOS transistor) or N (PMOS transistor).
- An insulating dielectric layer. It is usually SiO_2, or a high-K dielectric placed above an SiO_2 interfaced layer in advanced technologies.
- A commanding gate, which can be patterned in Poly-silicon or composed of a stack of metals in advanced technologies.
- Two highly doped charge tanks with a doping concentration of opposite type to the substrate called source and drain.

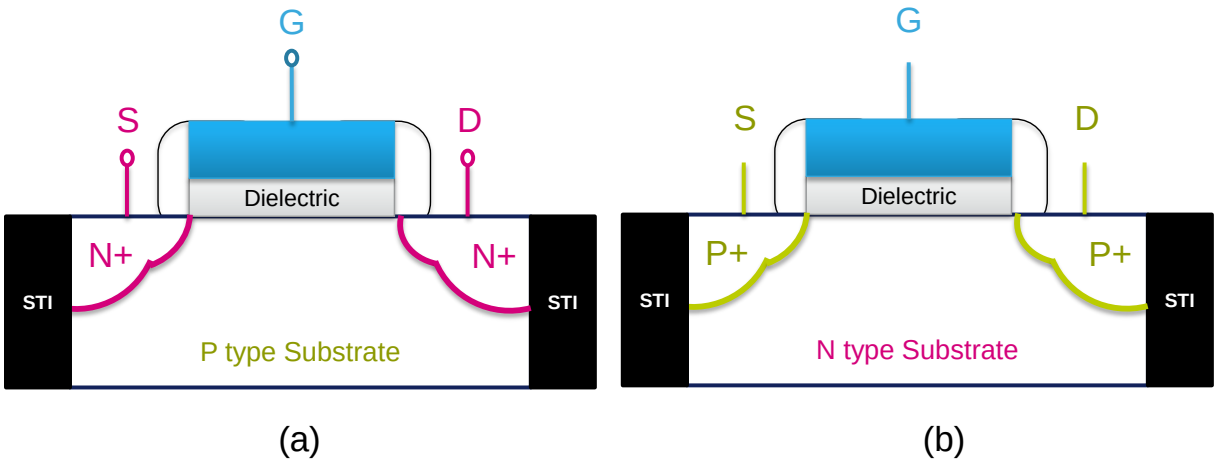


Figure I. 1: a) NMOSFET BULK transistor b) PMOSFET BULK transistor

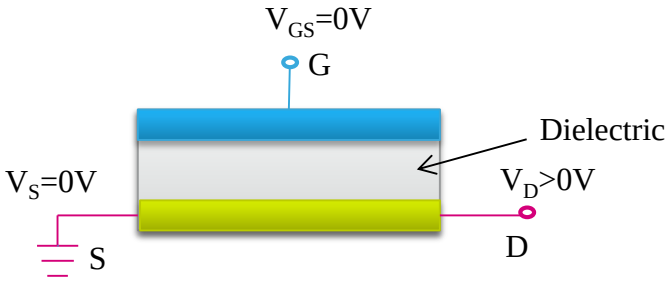
I.1.1 Operation principle

The operation of MOSFET transistors is based on the 'field' effect, where the local density of mobile charges in the semiconductor is electrostatically modulated by:

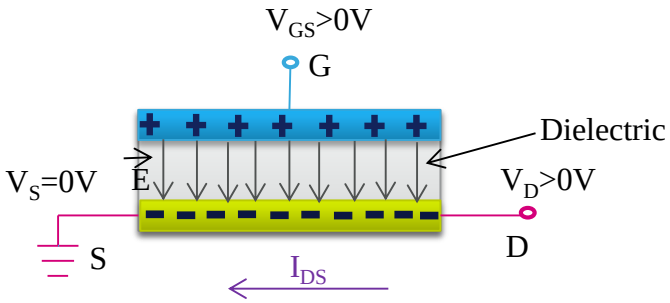
- Applying a potential difference between the Gate and the source (V_{GS}). This potential difference creates inversion charges (minority carriers) at the surface of the semi-conductor by a transversal field effect through the dielectric.

- Applying a potential difference between the source and the drain (V_{DS}). This potential difference allows the circulation of the minority carriers between the source and the drain and thus creates a drain current (I_D).

If the applied V_{GS} is lower than a potential called threshold voltage (*Vt*), the transistor is blocked and no current circulates between the source and the drain as shown in Figure I. 2.a. However, if V_{GS} is equal or higher than *Vt*, the minority carriers are modulated vertically to the surface of the semiconductor, and a region called channel is formed on the oxide/semi-conductor interface. The minority carriers can also be modulated horizontally by applying a V_{DS}, and thus forming a drain current that circulates between drain and source, as shown in Figure I. 2.b.



a- Empty channel => I_{DS}=0A=> Blocked channel



b- Channel filled of minority carriers => $I_{DS} \neq 0A$ => Passing channel

Figure I. 2 Example of Field effect in the case of NMOS transistor [Skotnicki03]

I.1.2 Electrical figures of merits for static performance

The performance of MOS transistors in static regime can be evaluated by measuring: the drain current when the transistor is in the open state (*Ioff*) (Blocked channel), the drain current when the transistor is in the closed state (*Ion*) (Passing channel), the sub-threshold swing (*SS*), the *Ion/Ioff* ratio and the threshold voltage (*Vt*), as shown in Figure I. 3.

- *Ioff* is measured between source and drain when V_{GS}=*0V, and* V_{DS}=V_{DD} *(NMOS) /* V_{DS}=-V_{DD} *(PMOS). Note that* V_{DD} *is the power supply voltage*. This current is mainly composed of the contributions of leakage currents between for instance the gate and the substrate, the gate and the drain, the gate and the source, the drain and the substrate, the source and the substrate. *Ioff* also depends on the amplitude of the potential barrier between the channel and the source/drain.
- *Ion* is measured between source and drain when V_{GS}=V_{DS}=V_{DD} *(NMOS)* or V_{GS}=V_{DS}=-V_{DD} *(PMOS).* This current is mainly modulated by V_{DS}. When V_{DS} is increased the drain current is also increased as shown in Figure I. 3.

The objective of an ideal transistor is to have an *Ioff* as low as possible, an *Ion* as high as possible and a transition between *Ioff* and *Ion* as abrupt as possible. This transition is characterized by the sub threshold swing (SS). Note that the theoretical limit of the sub threshold swing is of 60mV/decade at 300K of temperature. The *Ion/Ioff* ratio is mainly used as a single global performance parameter of the transistor. The higher the value of *Ion/Ioff*, the better the device. Finally, the threshold voltage (*Vt*) represents the barrier separating the blocked mode from the passing mode.

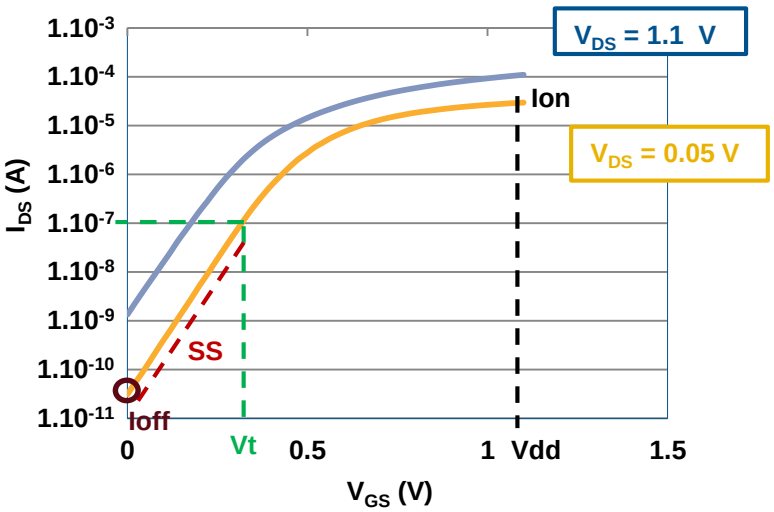


Figure I. 3 : ***$I_{DS}(V_{GS})$ characteristic for two different V_{DS} values (NMOS transistor).***

I.1.3 Operating Regimes

Considering the Metal/Oxide/Semiconductor structure (MOS capacitor), if a voltage (V_{GS}) is applied to the gate, the energy bands at the interface between the oxide and the

semiconductor bend. The MOS capacitor goes through different regimes as a function of the applied gate voltage.

We introduce:

- Φ_S: The potential at oxide/semi-conductor interface
- Φ_F: The Fermi potential, it represents the difference between the extrinsic Fermi level (for a doped semiconductor with acceptor doping N_A in the case of NMOS and donor doping N_D in the case of PMOS) and the intrinsic Fermi level (for the undoped semiconductor).
- Φ_m: The metal work function
- Φ_{SC}: The semiconductor work function
- V_{FB}: The flat band voltage, the required gate voltage to push Φ_S to 0, thus producing flat bands in the semiconductor. In the case of an ideal MOS transistor (no traps or charges in the oxide/semiconductor interface), V_{FB} is thus equal to the difference between (Φ_m) and (Φ_{SC}).

Adding the source and drain to the MOS capacitor, the difference of the types of doping between the substrate and the source/drain junctions creates a potential barrier Φ_D, where its height can also be modulated by the applied gate voltage.

The different operation regimes of the MOS transistor thus arise from the different applied gate voltages and consequently from the different values of Φ_S. Considering the case of NMOS transistors:

a- Accumulation regime: $V_{GS} < V_{FB} \Rightarrow \Phi_S < 0$

The energy bands of the semiconductor bend down as shown in Figure I. 4. The gate attracts holes from the substrate to the Oxide/Semiconductor interface. This phenomenon is called accumulation.

As a consequence, the potential barrier (Φ_D) is very high for the electrons present in the source to cross it. Even if a drain voltage (V_{DS}) is applied no drain current is observed.

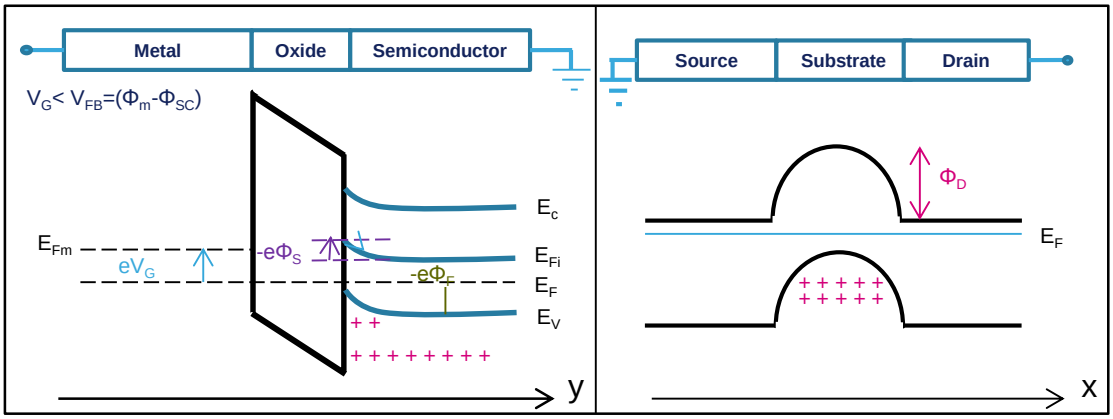


Figure I. 4 : Energy bands and potential barrier in Accumulation Regime (NMOS transistor) [Mathieu 01]

b- Flat band regime: $V_{GS} = V_{FB} = \Phi_m - \Phi_{SC} \Rightarrow \Phi_S = 0$

The energy band of the semi-conductor doesn't bend. The potential barrier (Φ_D) is still very high for the electrons present in the source to cross it as shown in Figure I. 5.

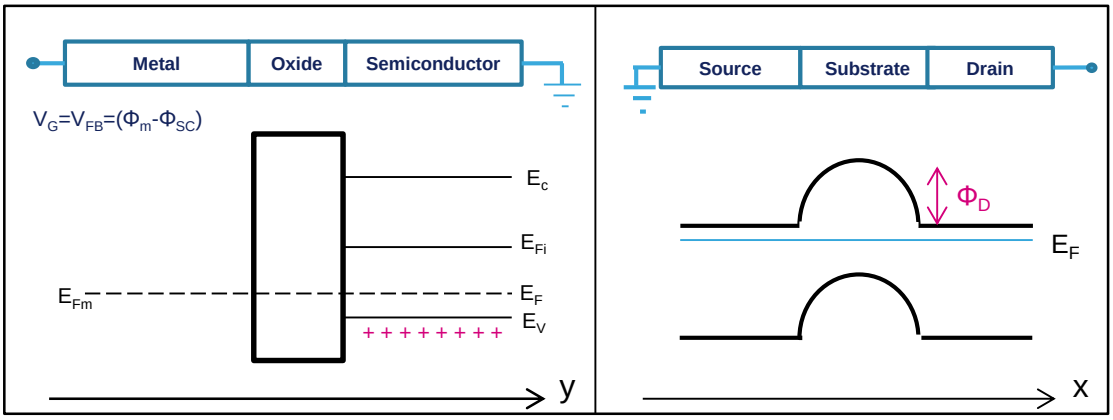


Figure I. 5 : Energy bands and potential barrier in Flat band Regime (NMOS transistor). [Mathieu 01]

c- Depletion regime: $V_{FB} = \Phi_m - \Phi_{SC} < V_{GS} < Vt \Rightarrow 0 < \Phi_S < \Phi_F$

The semiconductor energy bands bend upward as shown in Figure I. 6. The holes are rejected from the Oxide/Semiconductor interface to the substrate. An empty zone of mobile carriers is formed with a depletion charge *Qd*.

The potential barrier (Φ_D) starts to decrease, but is still too high for the electron to cross it. Also, in this case, even if a drain voltage (V_{DS}) is applied, no drain current is observed.

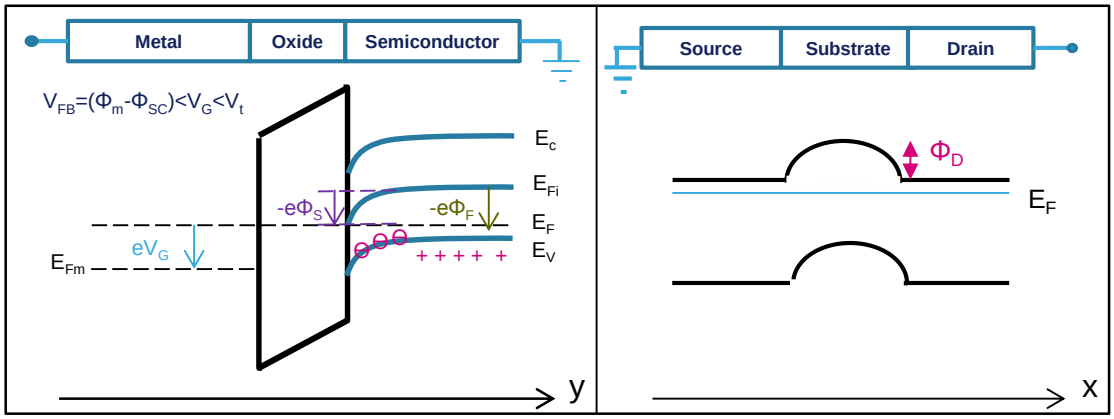


Figure I. 6: Energy bands and potential barrier in Depletion Regime (NMOS transistor). [Mathieu 01]

d- Inversion Regime:

- **Weak inversion regime:** $V_{FB} = \Phi_m - \Phi_{SC} < V_{GS} < Vt$ *and* $\Phi_F < \Phi_S < 2\Phi_F$

  The semiconductor energy bands bend more compared with the depletion regime and the potential barrier (Φ_D) height is thus decreased. Some electrons present in the source manage to cross Φ_D by thermal activation, and an inversion zone at the Oxide/Semiconductor interface starts to form. However the density of the electrons at the interface is lower than the density of the holes in the substrate. The electrons thus circulate due to a charge gradient (from the high concentration region, the Source, to the low concentration region, the drain). A diffusion drain current is thus formed that evolves exponentially with V_G.

  The threshold voltage (Vt) is defined as the voltage that causes the concentration of the electrons at the interface to be equal to the concentration of the holes in the substrate, in other term when $\Phi_S = 2\Phi_F$. This potential marks the state change of the transistor, which switches from weak to strong inversion regime. Vt can be expressed as shown in Equation I.1.

$$Vt = V_{FB} + 2\Phi_F - \frac{Qd}{Cox} \qquad \textbf{(I. 1)}$$

- **Strong inversion regime:** $V_{GS} > Vt$ *and* $\Phi_S > 2\Phi_F$

  The semiconductor energy bands bend in such a way that $\Phi_S > 2\Phi_F$. The potential barrier (Φ_D) drastically decreases and the electrons can easily cross the barrier as shown in Figure I. 7. The concentration of the electrons at the interface becomes much higher than the concentration of the holes in the substrate. The electrons can thus

circulate in the channel from the source to the drain due to the applied V_{DS}, following the drift-diffusion law.

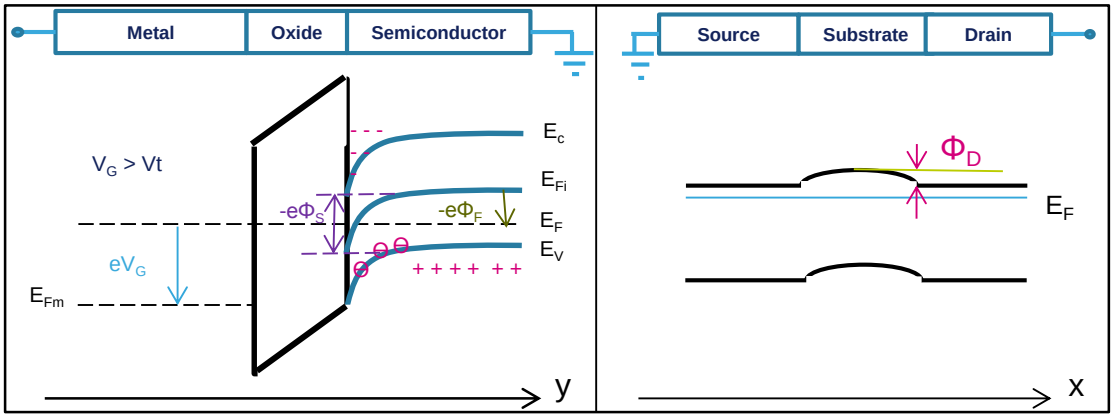


Figure I. 7 : Energy bands and potential barrier in Strong Inversion Regime (NMOS transistor) [Mathieu 01]

V_{DS} determines the regime of operation of the transistor. Three regimes can be observed: Linear, non-linear and saturation regimes.

We introduce the channel effective potential *Veff (x)*, where x is the coordinate that spans the length of the channel. At the source *(x=0)*, *Veff*=$V_{GS,}$ while at the drain *(x=d)*, *Veff*= V_{GS}-V_{DS}.

d.1 - Linear Regime: $V_{DS} < V_{GS} - Vt$

The channel is almost equipotential Veff(x=0) ≈ Veff(x=d) as shown in Figure I. 8.a.

- The electrons concentration is almost uniform along the channel
- The inversion channel extends over the entire area between the source and the drain

The MOS transistor operates like a resistor controlled by both the gate and the drain voltage. I_D increases linearly with V_{DS}, and is given by Equation I.2.

$$I_D = \beta.(V_{GS} - Vt - \frac{V_{DS}}{2}).V_{DS} \qquad \textbf{(I. 2)}$$

$$\beta = \frac{W}{L}\mu_0 Cox \qquad \textbf{(I. 3)}$$

,

where:

β is the current gain factor given by Equation I.3.

W is the transistor width

L is the transistor length

μ_0 is the low field mobility

Cox is gate oxide capacitance.

d.2 – Non-Linear or pinch off Regime: $V_{DS} = V_{GS} - Vt$

By increasing V_{DS}, the potential changes along the channel and is reduced considerably at the drain side, Veff(x=0) > Veff(x=d). The electrons concentration at the drain side is decreased, implying an augmentation of the channel electrical resistance. The drain current continues to increase with V_{DS}, but less rapidly than in the linear regime, until reaching the pinch off point P shown in Figure I. 8.b.

At the pinch-off point, saturation is achieved with $V_{DS} = V_{GS} - Vt$. The channel effective potential becomes equal to V_{GS} at the source and $V_{GS} - V_{GS} + Vt$ at the drain. This means that in the proximity of the drain the gate voltage is just enough to form the inversion layer and the electron concentration is almost negligible. The channel becomes more resistive and the drain current reaches saturation. Moreover, any higher potential applied to the drain will cause the channel effective potential at the drain side to be reduced below the threshold voltage and the region near the drain will be depleted.

d.3 - Saturation Regime: $V_{DS} \geq V_{GS} - Vt$

The region near the drain is not in strong inversion regime any more (Veff (x=d) < V_{GS} - V_{GS} + Vt), but rather in weak inversion regime. The electrons spread out and part of the channel is disconnected. While the depletion region lacks mobile carriers, there is no restriction on current flow through it: if an electron with initial velocity enters the depletion region from one side, and if there is a field across the region, this electron will be dragged by the field. The drain current is therefore quasi-independent of V_{DS} and is controlled only by V_{GS} and the $I_D(V_{DS})$ characteristic becomes flat, as shown in Figure I. 8.c. Note that when V_{DS} is increased, the pinch-off point moves towards the source and the channel length is decreased.

Considering $V_{DS,sat} = V_{GS} - Vt$, the saturation drain current can be written as Equation I.4:

$$I_D = \frac{\beta}{2}.(V_{GS} - Vt)^2 \qquad \textbf{(I. 4)}$$

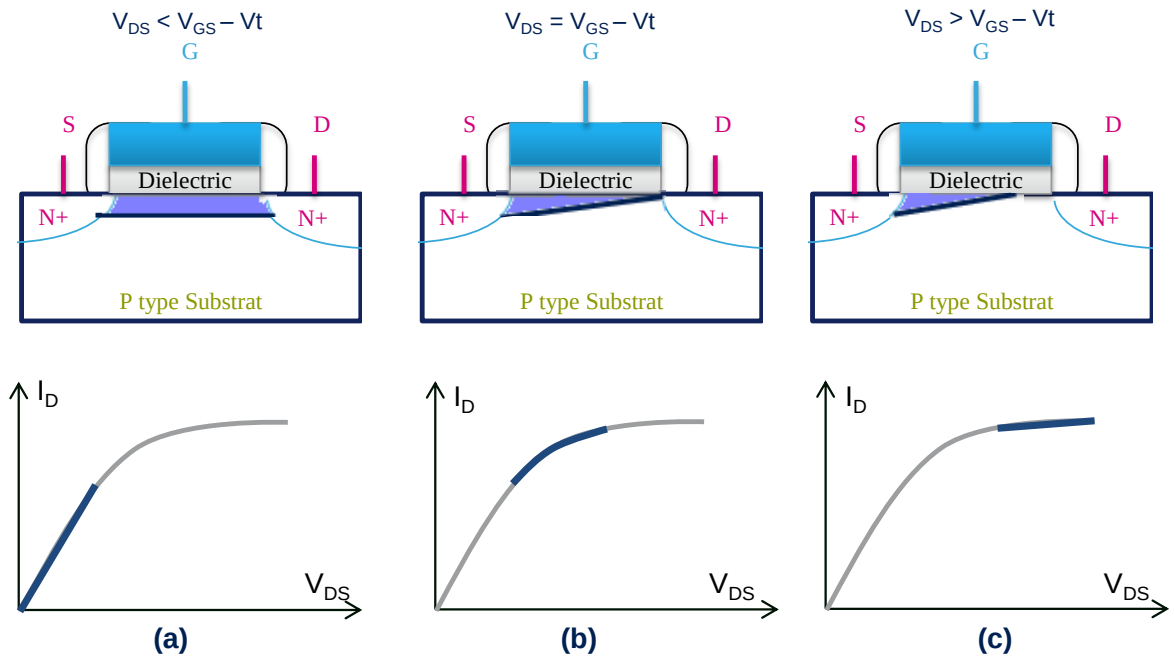


Figure I. 8 : Energy bands and potential barrier in Strong Inversion Regime (NMOS transistor) [Skotnicki03]

I.1.4 Parasitic effects due to the Miniaturization of MOS transistors

In 1975 Gordon Moore predicted that the numbers of transistors in circuits of a given size will double every two years, allowing an exponential performance enhancement. The miniaturization of MOS transistors that enables the increase in device number per area unit allows the saturation current to be high enough to increase the operating speed of the products. The challenge in this case is to prevent disruptive increase of leakage currents, in order to limit the power consumption of these products, especially if battery powered.

The miniaturization of MOS transistors also induces parasitic phenomena, disrupting the electrical operation of ideal devices and it is necessary to understand and control such effects. In this paragraph, we introduce the main parasitic effects encountered and mentioned in this work and some of their control techniques.

1- Short channel effect (SCE) and Drain induced barrier Lowering (DIBL).

In real devices, the n/p junctions between the source/drain extensions and the channel are not abrupt. These junctions create depleted zones (depletion charge) of a few nanometers uncontrolled by the gate polarization. In these regions called Space Charge Zones (SCZ), the potential is decreased in a quadratic fashion.

- Linear regime.

- For long transistors, the surface potential is constant along the channel except near the source and the drain junctions due to the SCZs, as shown in Figure I. 9.a.
- For short transistors, the SCZs approach each other with the reduction of the gate length, until they are partly overlapped. In this case, the flat behavior of the surface potential noticed for long transistors is no more observed, as shown in Figure I. 9.b. The depletion charge in the channel is not completely controlled by the gate polarization but majorly by the junction zones. The potential barrier (Φ_D) is thus decreased. As a consequence the inversion regime is quickly reached and *Vt* is lowered. This phenomenon is called short channel effect (SCE).

- Saturation regime.

  In addition to the SCE, when polarizing the drain with a strong drain field the potential barrier will also decrease as shown in Figure I. 9.c. This phenomenon, called Drain Induced Barrier Lowering (DIBL), induces a further lowering of Vt compared to the case of linear regime shown in Figure I. 10.a and b.

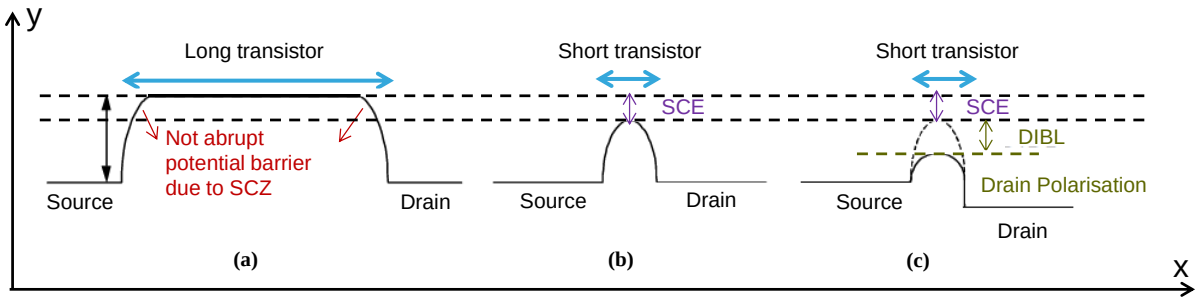


Figure I. 9: Surface potential in Strong Inversion Regime as a function of transistor length (NMOS transistor) [Skotnicki03][Gallon 07]

SCE and DIBL denote a loss of the electrostatic control of the channel by the gate, due to the miniaturization of the channel length. The gate modulation of the channel potential barrier in less efficient, implying a degradation of *SS*. The uncontrolled decrease of the potential barrier will induce an uncontrolled lowering of the threshold voltage *Vt*, and a significant degradation of *Ioff* as shown in Figure I. 10.b.

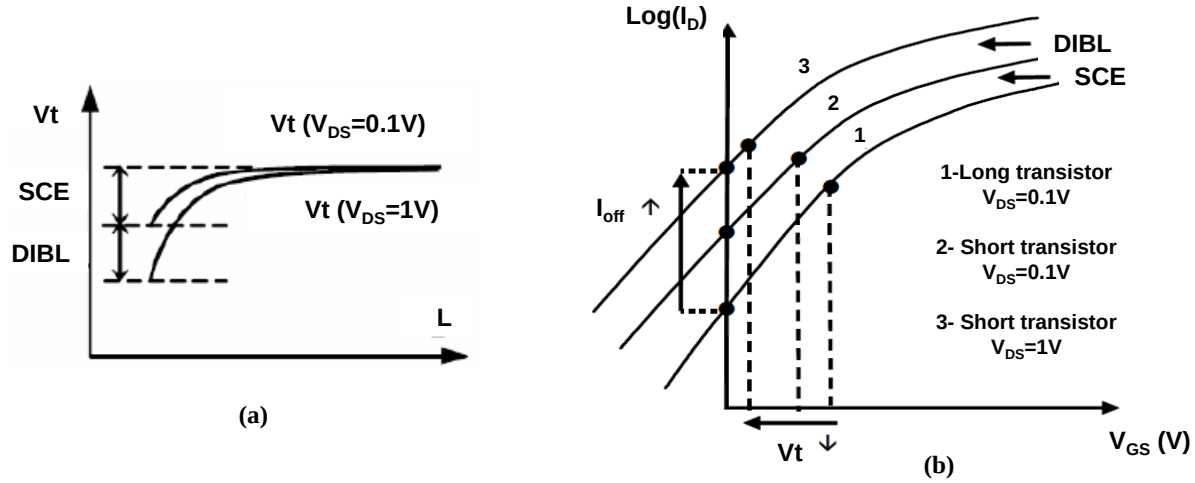


Figure I. 10: Short channel effect and Drain induced barrier lowering effect on (a) threshold voltage as a function of L and (b) $I_D(V_{GS})$ characteristic for long and short devices [Skotnicki03][Gallon 07]

The SCZ mainly extends a few nanometers in the channel, due to its low doping as compared to the source/drain. To eliminate the SCE and DIBL effects, two highly doped regions called pockets or halo, having the same doping type as the substrate, are implanted near the source and the drain as shown in Figure I. 11. This pocket implantation limits the extension of the SCZ and thus of the SCE.

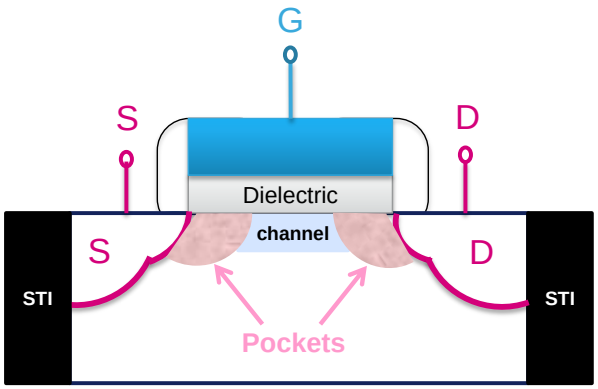


Figure I. 11: Transistor NMOS with pocket implant

For small gate lengths, the pocket regions are close to each other's forming a homogenous channel controlled by the gate polarization. As the pockets are highly doped, the channel doping is increased, increasing the potential barrier and thus *Vt*. This phenomenon is called reverse short channel effect.

2- Gate leakage due to the reduction of the oxide thickness (*Tox*).

In the purpose of granting sufficient drain current, it is important to maintain high Cox value as shown in Equations I.2, I.3 and I.4. The traditional technique to improve the

capacitive coupling between the gate and the channel is to reduce the oxide thickness (*Tox*). However, by decreasing the oxide thickness to a few Angstroms, it becomes more probable for the minority carriers to cross the potential barrier of the dielectric. A leakage gate current can be observed between the gate and the substrate and the gate and the source drain extensions. To face this issue, the silicon dioxide is replaced by a high-k material in advanced technologies such as HfO_2 and HfSiON. This enables larger oxide thickness for a given target Cox value, limiting therefore the gate leakage.

The high-k layer is usually deposited on a SiO_2 interfacial layer. As a consequence, instead of considering the oxide thickness *Tox* as in the case of simple silicon dioxide dielectric, an equivalent oxide thickness *(EOT)* is considered, equal to the sum of the contributions of the SiO_2 interfacial layer and the high-k dielectric layer.

3- Increasing EOT due to Poly-Silicon Gate

The Poly-Silicon gate is known to induce a depletion layer between the gate itself and the oxide, thus increasing the EOT. One of the main solutions to this problem is the use of a metal gate. The metal gate technology, even with its difficulty of integration (compatibility with the gate oxide, chemical contamination, etc. [Tavel 01]) has another advantage over the poly-silicon technology, which is given by its low resistivity. This enables a decrease of the delay in signal propagation in high frequency applications.

By using a metal gate, the threshold voltage will be dependent of the gate material through V_{FB} ($V_{FB} = \Phi_m - \Phi_{SC}$)**.**

I.2 Methodology of extraction of MOS transistors parameters

The development of MOS transistors technology leads to additional complexities that make the calculation of its electrical parameters increasingly difficult. Several methods for measuring these electrical parameters under static conditions exist, meeting various constraints such as repeatability, ease and speed of measurement and reliability.

While the drain current (I_D) can be directly extracted for a known gate and drain voltage, the extraction of the threshold voltage (*Vt*) and current gain factor (β) is more complex. Some of the most known and used methods to extract these two parameters are the constant current

method [Deen 90], the maximum slope method [Hao 85], the three-point method [Hamer 86], the Y function method [Ghibaudo 88] and the shift & ratio method [Taur 92].

In this thesis the constant current, maximum slope and Y function methods are used and thus detailed below.

I.2.1 Maximum slope method

The drain current I_D is measured as a function of gate bias (V_{GS}) in linear regime. The Trans-conductance (Gm) is then calculated using Equation I.5.

$$Gm = \frac{\partial I_D}{\partial V_{GS}} \qquad \textbf{(I. 5)}$$

I_D and Gm are plotted as a function of V_{GS}, as shown in Figure I. 12 with drain bias $V_{DS} = 50mV$.

As shown in Figure I. 12, the maximum value of Gm (y = G_{mMax}) and the inflection point (y = $I_D\big|_{GmMax}$) of the $I_D(V_{GS})$ characteristic are obtained for the same gate bias $V_{GS}\big|_{GmMax}$. Note that the inflection point marks the transition of MOS transistor from weak to strong inversion regime. The current gain factor $\beta_{extrapolated}$ can thus be extracted at the maximum Gm point using Equation I.6, while the threshold voltage $Vt_{extrapolated}$ can be extracted using Equation I.7.

$$\beta_{extrapolated} = \frac{G_{m.Max}}{V_{DS}} \qquad \textbf{(I. 6)}$$

$$Vt_{extrapolated} = V_{GS}\big|_{GmMax} - \frac{I_D\big|_{GmMax}}{G_{mMax}} \qquad \textbf{(I. 7)}$$

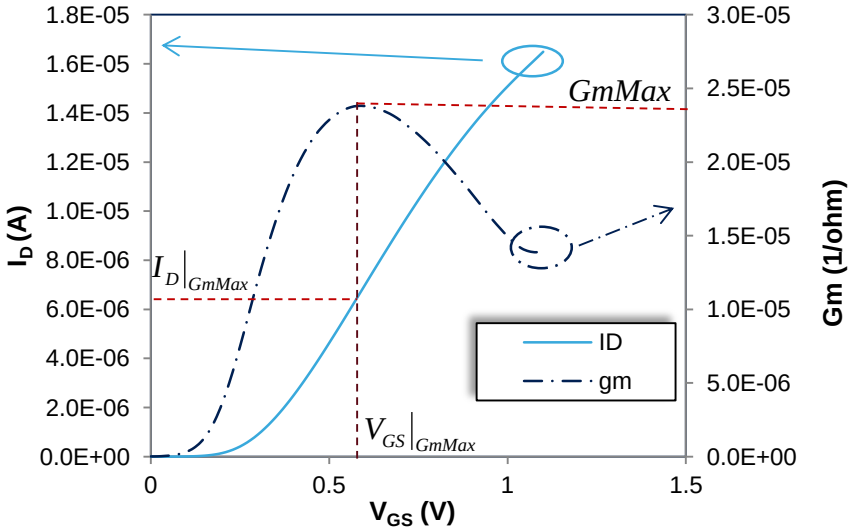


Figure I. 12 : Maximum slope method for linear regime (V_{GS}=1.1V, V_{DS}=50mV), for Bulk transistors with W=0.135µm and L=0.04µm

This is a reproducible method that gives a physical value of threshold voltage [Ghibaudo 89]. However, [Ghibaudo 89] shows that this value depends on the mobility attenuation factor θ_1. If θ_1 is large, the extrapolated *Vt* can deviate from the real *Vt* value as shown in Equation I.8.

$$Vt_{extrapolaed} = Vt - \theta_1.(V_{GS}|_{GmMax} - Vt)^2 \qquad \textbf{(I. 8)}$$

Although a method has been demonstrated at a later stage [Shimizu 02] to extract *Vt* and β in saturation regime, the values of *Vt* and β used in this thesis were extracted in linear regime.

I.2.2 Constant current method

The threshold voltage is defined as the necessary gate voltage to obtain a defined current level *Icc* as shown in Equation I.9.

$$Icc = I_{Normalized}.\frac{W}{L} \qquad \textbf{(I. 9)}$$

Usually, the normalized current is defined in weak inversion mode, where the drain current equation follows an exponential law as a function of V_G.

The constant current method is faster than the maximum slope method. Indeed, while the maximum slope method is based on scanning the $gm(V_{GS})$ curve to find the maximum

slope, the constant current method is based on classical interpolation extractions such as dichotomy, and thus requires less measurement points. This method is also reproducible and can be used in linear and saturation regimes as shown in Figure I. 13.

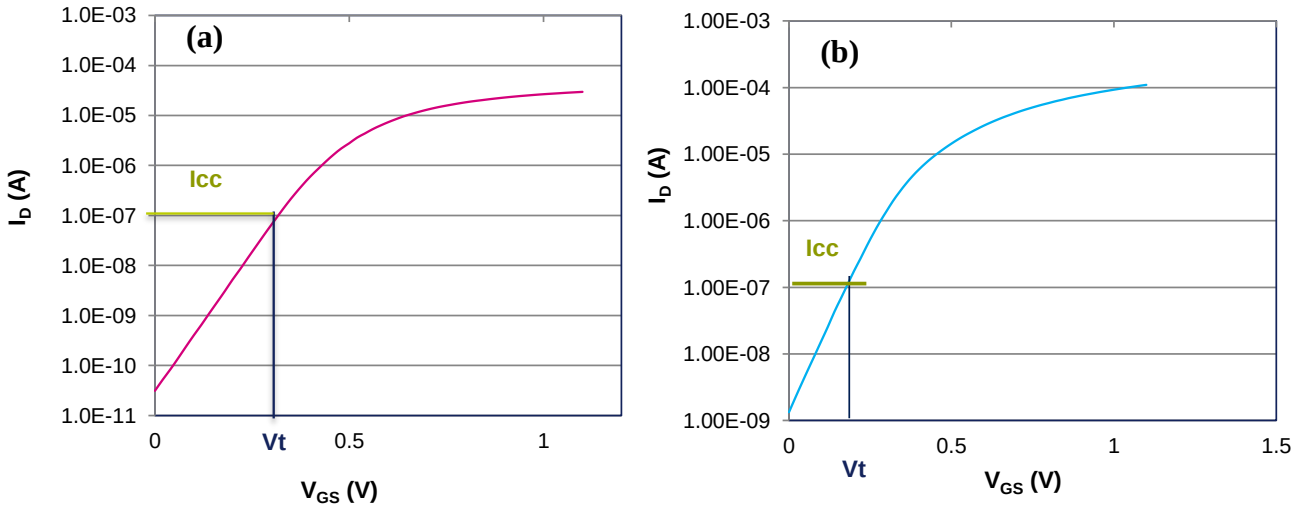


Figure I. 13: Constant current method for (a) linear regime (V_{GS}=1.1V, V_{DS}=50mV) and (b) saturation regime (V_{GS}=1.1V, V_{DS}=1.1V), for Bulk transistors with W=0.135µm and L=0.04µm

The disadvantage of this method is that it only enable the extraction of *Vt* values.

I.2.3 Y function method

The drain current equation as a function of V_G, in linear regime, can be written as shown in Equation I.10.

$$I_D = \frac{W}{L}.\mu_0.C_{OX}\frac{V_G - Vt}{1+\theta_1.(V_G - Vt)+\theta_2.(V_G - V_T)^2}.V_D \qquad \textbf{(I. 10)}$$

Where θ_1 (defined in Equation I.11 where $\theta_{1,0}$ is the intrinsic mobility reduction factor) and θ_2 are the mobility attenuation factors, and β is the current gain factor (defined in Equation I.12).

$$\theta_1 = \theta_{1,0} + \beta.Rsd \qquad \textbf{(I. 11)}$$

$$\beta = \frac{W}{L}.\mu_0.C_{OX} \qquad \textbf{(I. 12)}$$

As shown in Equation I.11, θ_1 depends on *Rsd* values. For short gate lengths *Rsd* has an large impact on the values of I_D in strong inversion regime, as shown in Figure I. 14. It is thus mandatory to extract *Vt* and β values in a method that overcomes the influence of *Rsd*.

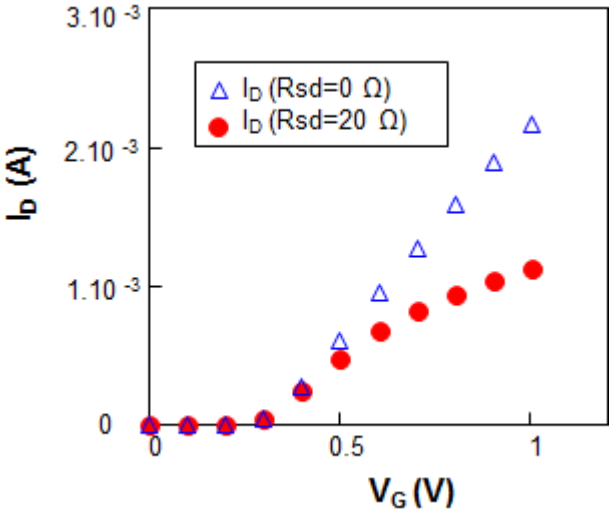


Figure I. 14 : Calculated drain current values as a function of gate voltage, for Rsd=20Ω and Rsd=0Ω. (FD SOI transistors with W=0.08µm/L=0.05µm and V_D =50mV).

The *Y* function given by Equation I.13, which has been introduced as a simple method to extract the MOS transistor's parameters [Ghibaudo88] & [Fleury08], is immune to *Rsd* values as shown in Figure I. 15.

$$Y = \frac{I_D}{\sqrt{Gm}} \qquad \textbf{(I. 13)}$$

The trans-conductance *Gm* is defined as

$$Gm = \frac{\partial I_D}{\partial V_G} = \frac{W}{L}.\mu_0.C_{OX}\frac{V_D}{(1+\theta_1.(V_G - Vt))^2}, \qquad \textbf{(I. 14)}$$

so that the *Y* function can be written as shown in Equation I.15

$$Y = \frac{I_D}{\sqrt{Gm}} = \sqrt{\frac{W}{L}Cox\mu_0 V_D}.(V_G - Vt) \textbf{ if } \theta_2 = 0 \qquad \textbf{(I. 15)}$$

Note that in practice $\theta_2 \approx 0$ except for very high V_G values [Fleury08].

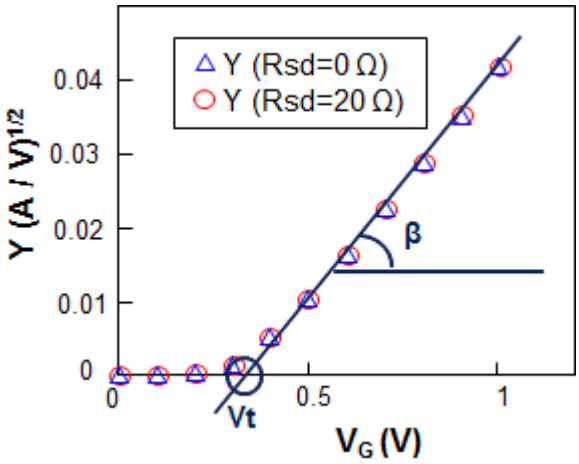


Figure I. 15: Calculated Y function values as a function of gate voltage, for Rsd=20Ω and Rsd=0Ω. (FD SOI transistors with W=0.08µm/L=0.05µm and V_D =50mV).

In strong inversion regime, the $Y(V_G)$ characteristic varies linearly with V_G as shown in Figure I. 15. It is thus easy to extract the threshold voltage value by extrapolating the value at $Y=0$ of the linear portion of the $Y(V_G)$ curve, as shown in Figure I. 15. Moreover, the current gain factor (β) can also be extracted by calculating the slope of the linear region of $Y(V_G)$.

I.3 Types of electrical variability

When measuring the electrical variability of MOS transistors between two factories, two lots, two wafers or two separate dies, the global devices variability is characterized as shown in Figure I. 16. Often, this global variability is due to different fabrication processes, such as the use of different fabrication tools between two factories or the temperature gradient effect during the oxidation or annealing steps of the back end fabrication. In contrast, the local devices variability, also called mismatch, is characterized by measuring two identical MOS devices:

- Placed in pairs
- Spaced by the minimum allowed distance
- Laid out in identical environment
- Electrically independent with symmetric connections

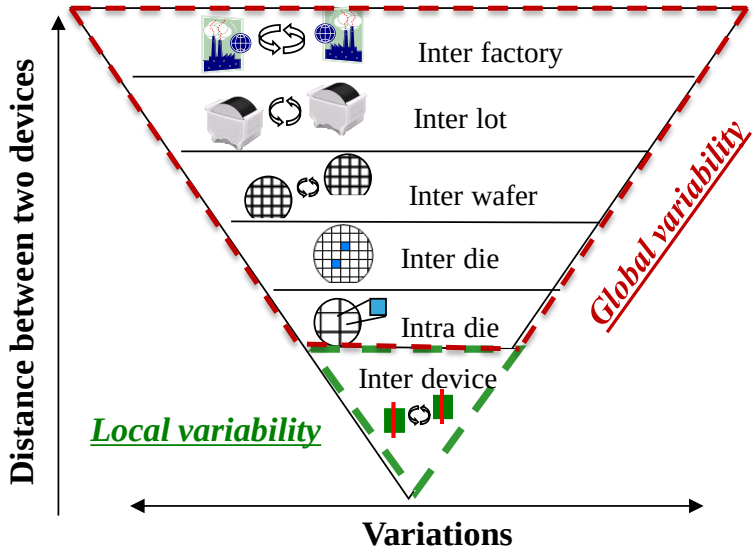


Figure I. 16 : Different types of electrical variability [Mezzomo10b][Croon 04]

I.4 Local variability

We will first introduce the concept of statistical local variability computation, allowing the decomposition of the local variability into systematic and stochastic mismatch. Then we will define each type of variability and we will mostly concentrate on the stochastic mismatch.

I.4.1 Measurement phase

With the aim of measuring the local variability, a 300mm wafer is considered as an example. The measurements are conducted on two identical devices (MOS transistors in this case) within the same die. The electrical parameter P_1 of device1 (MOS1) and the electrical parameter P_2 of device2 (MOS2) are measured, then ΔP or $\frac{\Delta P}{P}$ are calculated as shown in Figure I. 17.

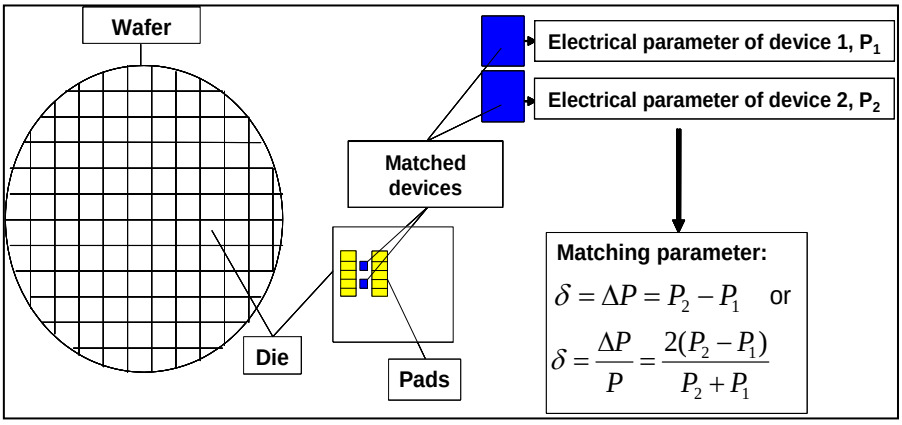


Figure I. 17: Measurement of the electrical parameters P1 and P2 for a pair of devices

This measurement is repeated for N pairs of MOS transistors. A large number of transistors in pairs (70 pairs and above) are considered to assure a significant statistical population.

I.4.2 Gaussian distribution verification

I.4.2.a Data plot

When the N samples of ΔP or $\frac{\Delta P}{P}$ are plotted as a function of their number of occurrence, a Gaussian shape is usually obtained as shown in Figure I. 18.

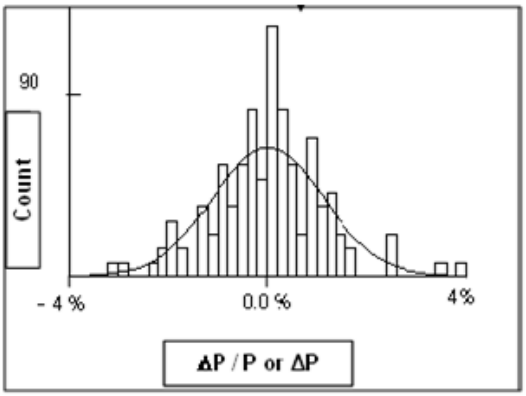


Figure I. 18: An example of statistical plot of the number of occurrences of each measured value of ΔP or $\frac{\Delta P}{P}$

This Gaussian plot is characterized by its mean value ($\overline{\Delta P}$ or $\overline{\frac{\Delta P}{P}}$) (Equation I.16) and its standard deviation ($\sigma_{\Delta P}$ or $\sigma_{\frac{\Delta P}{P}}$) (Equation I.17).

$$\overline{\Delta P} = \frac{1}{N}\sum_{i=1}^{N} \Delta P \qquad \textbf{(I. 16)}$$

$$\sigma_{\Delta P} = \sqrt{\frac{1}{N-1}.\sum_{i=1}^{N}(\Delta P - \overline{\Delta P})^2} \qquad \textbf{(I. 17)}$$

I.4.2.b Gaussian law verification

Theoretically, considering a finite number of samples, the random measured variable ΔP or $\frac{\Delta P}{P}$ is Gaussian if its probability density function is of the form:

$$f(\Delta P) = \frac{1}{\sigma_{\Delta P}.\sqrt{2.\pi}} \exp(-\frac{(\Delta P - \overline{\Delta P})^2}{2.\sigma_{\Delta P}^2}) \qquad \textbf{(I. 18)}$$

In practice, however, even if considering an important number of samples, the experimental data doesn't perfectly follow this law. Thus, a test to verify that the experimental distribution matches the normal law is mandatory. The chi-squared test enables to validate or to reject the Gaussian distribution.

To explain how this test works, the hypothesis H is first considered: the distribution of the experimental data is Gaussian.

The χ^2 function expresses the difference between:

- the observed (O_i) frequency of occurrence of the measured data
- the expected (E) frequency of occurrence of the data calculated using Equation I.18

χ^2 is defined as:

$$\chi^2 = \sum_{i=1}^{k} \frac{(Oi - Ei)^2}{Ei} \qquad \textbf{(I. 19)}$$

where k represents the number of classes (the number of intervals over which the distribution is divided to determine the frequency of occurrence: [$\Delta P_i - \Delta P_{i-1}$]).

To verify the H hypothesis, an assessment parameter χ_α^2 must be defined, which depends on the confidence level $(1-\alpha)$ and on the degrees of freedom ν [Montgomery01], with

$$\nu = k - m - 1 \qquad \textbf{(I. 20)}$$

where m represents the number of parameters to be determined and k is chosen from the Cochran criterion [Cochran54], which states that all classes should have a theoretical non-zero value and 80% of the classes should have a theoretical value greater than or equal to 5. In our

case k = 56 and m = 2 (2 parameters, $\overline{\Delta P}$ and $\sigma_{\Delta P}$), thus $\nu > 30$. χ_α^2 can in this case be written as shown in Equation I.21:

$$\chi_\alpha^2 = \frac{1}{2}.(Z_\alpha + \sqrt{2\nu - 1})^2 \qquad \textbf{(I. 21)}$$

where Z_α represents the standard deviation number from the normal central limit theorem and can be extracted from Table I.1 below.

Table I.1: *Z_α values of the central limit theorem*

$(1-\alpha)$	99.73%	99%	98%	96%	95.45%	95%	90%	80%	68.27%	50%
Z_α	3	2.58	2.33	2.05	2	1.96	1.645	1.28	1	0.6745

In our case we consider a restricted interval $\left[\overline{\Delta P} - 3\sigma_{\Delta P}; \overline{\Delta P} + 3\sigma_{\Delta P}\right]$, thus our confidence level is 99%, and consequently $Z_\alpha = 2.58$.

Once all parameters have been evaluated, the test requires to verify whether $\chi^2 < \chi_\alpha^2$, in which case H will be accepted, else H will be rejected.

The chi-squared test methodology can therefore be conducted on our data to identify whether it follows a Gaussian distribution or not.

I.4.3 Data filtering and separation between systematic and stochastic mismatch

The experimental data must be filtered to exclude erroneous values arising from measurement errors such as high probe resistance [Cathignol07], or technology defects during MOS transistor fabrication. After verifying that the data follows a Gaussian law, and computing the mean and the standard deviation, a recursive filter is applied to obtained ΔP or $\frac{\Delta P}{P}$ values. The used filter is of iterative type: it selects only the values between $\overline{\Delta P} \pm 3.\sigma_{\Delta P}$ with a 99% probability of occurrence, and repeats this action until no values of ΔP or $\frac{\Delta P}{P}$ outside $\overline{\Delta P} \pm 3.\sigma_{\Delta P}$ are present, as shown in Figure I. 19.

After eliminating all the erroneous data, a final estimation of $\overline{\Delta P}$ and $\sigma_{\Delta P}$ is calculated. At this point a separation between stochastic and systematic mismatches can be introduced by associating $\overline{\Delta P}$ to systematic mismatch and $\sigma_{\Delta P}$ to stochastic mismatch.

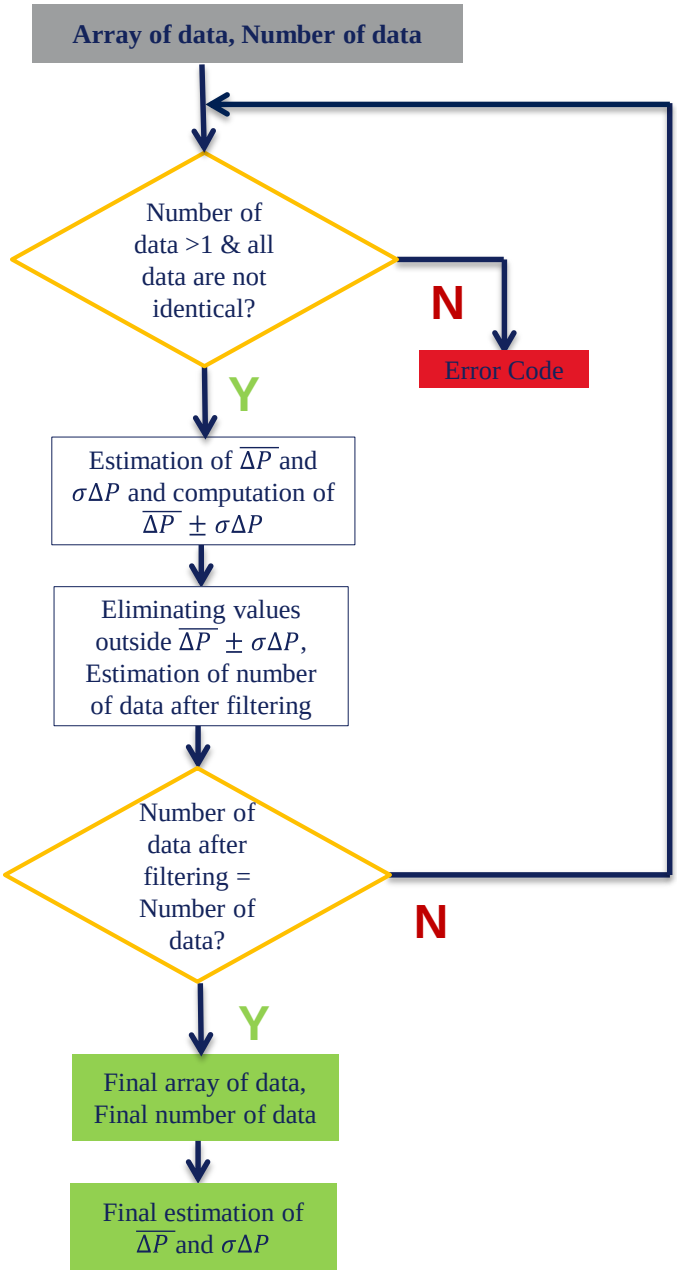


Figure I. 19: Scheme of recursive filter

I.4.4 Concept and computation of systematic mismatch

I.4.4.a Concept of systematic mismatch

Systematic mismatch is mainly caused by the difference in the environment where the pair of examined devices is laid out. Tuinhout in [Tuinhout96] [Tuinhout97b] explained that systematic mismatch arises mainly due to inadequate design practices For example, the use of a metallic cover over only one device of the pair can induce local differences in terms of mechanical constraints, which in turn induce systematic mismatch. The same author also identified in [Tuinhout03] the phenomena that can induce differences in the measurement

conditions for the pair of devices, thus inducing systematic mismatches. As systematic mismatch is mostly due to design factors, it can also be reduced by following more mismatch-aware practices. One of the techniques to reduce this kind of local variability is the use of dummies in MOS transistors conception. Dummy devices are not connected to the pair of transistors, but are placed on both sides of the gate to assure the same surrounding environment for both transistors of the pair.

I.4.4.b Systematic mismatch computation

Systematic mismatch is usually considered to be negligible compared to stochastic mismatch. To validate this hypothesis, a zero-mean test is considered.

This test is used to validate or reject the following hypothesis:

- H: the experimental values follow a Gaussian distribution with $\overline{\Delta P} = 0$.

For this test, the reduced centered variable of [Pergoot95] for a confidence level of $1-K = 99\%$ is considered, defined as:

$$Z = \frac{\overline{\Delta P}}{\sqrt{\frac{2.\sigma_{\Delta P}^2}{N}}} \qquad \textbf{(I. 22)}$$

where N is the number of samples.

The comparison parameter for this test is $Z_{k/2}$, which for $K = 1\%$ is equal to 2.58.

Based on these parameters, if $Z \leq Z_{K/2}$, H will be accepted and the systematic mismatch can be deemed negligible, else H is rejected.

I.4.4.c Confidence interval

In practice, a finite sample of random variables is considered, thus the mean and the standard deviation of the Gaussian law represent estimated values of the real ones. These estimated values have a small probability to coincide with the real ones. A confidence interval is therefore introduced, mainly based on the estimated values of $\overline{\Delta P}$ and $\sigma_{\Delta P}$ and on the number of samples considered. The confidence interval so defined guarantees that the real value (the mean in this case) falls within the identified interval with a confidence level of $1-K(\%)$.

For numbers of samples greater than 30, the real mean value follows a normal central limit theorem and falls in the confidence interval

$$\overline{\Delta P} - Z_{K/2} \cdot \frac{\sigma_{\Delta P}}{\sqrt{N}} < \overline{\Delta P}_{Reel} < \overline{\Delta P} + Z_{K/2} \cdot \frac{\sigma_{\Delta P}}{\sqrt{N}} \qquad \textbf{(I. 23)}$$

I.4.5 Stochastic mismatch

I.4.5.a Concept and computation of stochastic mismatch

For correct operation, analogue and digital applications such as power amplifiers or Static Random Access Memories (SRAM) cells require pairs of identical transistor devices. The two MOS of the pair should be identically designed and laid out in an identical environment in order to ensure identical electrical performance. Real devices, however, suffer from variations in the electrical parameters, a problem known as mismatch.

While well know design solutions exist to improve systematic mismatch, intrinsic sources of random dispersions exist within the devices, arising from stochastic variations inherent to the discrete nature of dopant impurities, point defects, or, more generally, due to the random nature of processing steps.

The first mismatch studies were conducted in 1972 by Hoeneisen and Mead [Hoeneisen72]. The authors observed that random dopant fluctuation in the MOSFET's body can result in unpredictable threshold voltage values, and that such unpredictability can gravely hinder advances in MOSFET technologies. The same problem was also studied by Keyes [Keyes75] whose work was focused on the creation of a model to predict the amplitude of the threshold voltage variations, without considering the MOSFET operation. Shyu *et al*. also created a complete mismatch model for MOS capacitors and MOS transistors [Shyu84] by considering as source of variability the fluctuations in the physical dimensions of the active zone and in the process parameters. Based on this model, Lakshmikumar *et al*. experimentally demonstrated the dimensional dependence of mismatch in MOS devices [Lakshmikumar86]. In 1989 Pelgrom *et al*. indicated a direct dependency between the local fluctuations of an electrical parameter *P* and the channel area (denoted as *S*) through a coefficient *A* [Pelgrom89]. This is known as Pelgrom's Law, expressed in Equation I.24.

$$\sigma_{\Delta P} = \frac{A}{\sqrt{S}} \qquad \textbf{(I. 24)}$$

These preliminary studies, in combination with the miniaturization of MOSFET devices, have set the ground for increasing research efforts aimed at achieving a deeper understanding of the causes of mismatch phenomena and characterizing their effects, with the objective of guaranteeing reliable integrated circuits performance.

I.4.5.b Confidence interval

Considering a finite sample of random variables, the mean and the standard deviation of a Gaussian law represent estimated values of the real quantities. Such estimated values have a small probability to coincide with the real values. A confidence interval is thus introduced, mainly based on the estimated $\sigma_{\Delta P}$ values and on the number of samples considered. The confidence interval so defined guarantees that the real value (the standard deviation in this case) falls within the identified interval with a confidence level of $(1-\gamma)\% = 99\%$. Using the approach proposed by Pergoot [Pergoot95], it is possible to state that the real value of the standard deviation can fall within the confidence interval expressed in Equation I.25.

$$\frac{\sigma_{\Delta P}.\sqrt{N-1}}{\chi_{1-\gamma/2}} < \sigma_{\Delta P\,Reel} < \frac{\sigma_{\Delta P}.\sqrt{N-1}}{\chi_{\gamma/2}} \qquad \textbf{(I. 25)}$$

The upper and lower standard deviation limits can be obtained by writing Equation I.25 as follows:

$$\sigma_{\Delta P}.(1-Y) < \sigma_{\Delta P\,Reel} < \sigma_{\Delta P}.(1+X) \qquad \textbf{(I. 26)}$$

where:

$$X = 1+\sqrt{\frac{N-1}{\chi^2_{\gamma/2}}} \qquad \textbf{(I. 27)}$$

$$Y = 1-\sqrt{\frac{N-1}{\chi^2_{1-\gamma/2}}} \qquad \textbf{(I. 28)}$$

Table I.2 lists examples of errors (upper and lower uncertainity limits) and the confidence level on the estimated standard deviation for a given number of samples. The table shows that when the number of samples increases, the uncertainity decreases. The values also shows a

dyssimetry between upper and lower uncertainity limits, that can be reduced when the number of samples is increased. This highlights the importance of using large numbers of samples.

Table I.2: *Upper and lower confidence limits for a confidence levels of 99%.*

Number of samples	Upper Uncertainty (%)	Lower Uncertainty (%)	Average Uncertainty (%)
10	127.8	38.2	83.0
20	66.6	29.8	48.2
30	48.7	25.6	37.1
40	39.7	22.8	31.2
50	34.1	20.9	27.5
60	30.3	19.4	24.8
70	27.4	18.2	22.8
80	25.2	17.2	21.2
90	23.5	16.3	19.9
100	22.0	15.6	18.8
120	19.7	14.4	17.1
140	18.0	13.5	15.7
160	16.7	12.7	14.7
180	15.6	12.1	13.8
200	14.7	11.5	13.1
300	11.7	9.6	10.6
400	10.0	8.4	9.2

I.4.5.c Deviations from Pelgrom's Law

With the miniaturization of MOS transistors, different phenomena affecting the Vt values are observed such as the SCE or the effect of pocket implants in the channel. These phenomena may cause various deviations from Pelgrom's law, such as variations in the A parameter (not any more a constant, [Stolk98], [Croon02b] and [Rochereau04]). An individual constant of matching ($iA_{\Delta P}$) is thus introduced. This new parameter allows the evaluation of the mismatch values for each channel dimension as shown in Equation I.29.

$$iA_{\Delta P} = \sigma_{\Delta P}.\sqrt{W.L} \qquad \textbf{(I. 29)}$$

This parameter will be the main object of investigation for the characterization work reported in this thesis.

I.5 Mismatch measurement system and test structures

I.5.1 Mismatch measurement system

Electrical characterization and reliability measurements require special equipment, such as the system depicted in Figure I. 20.

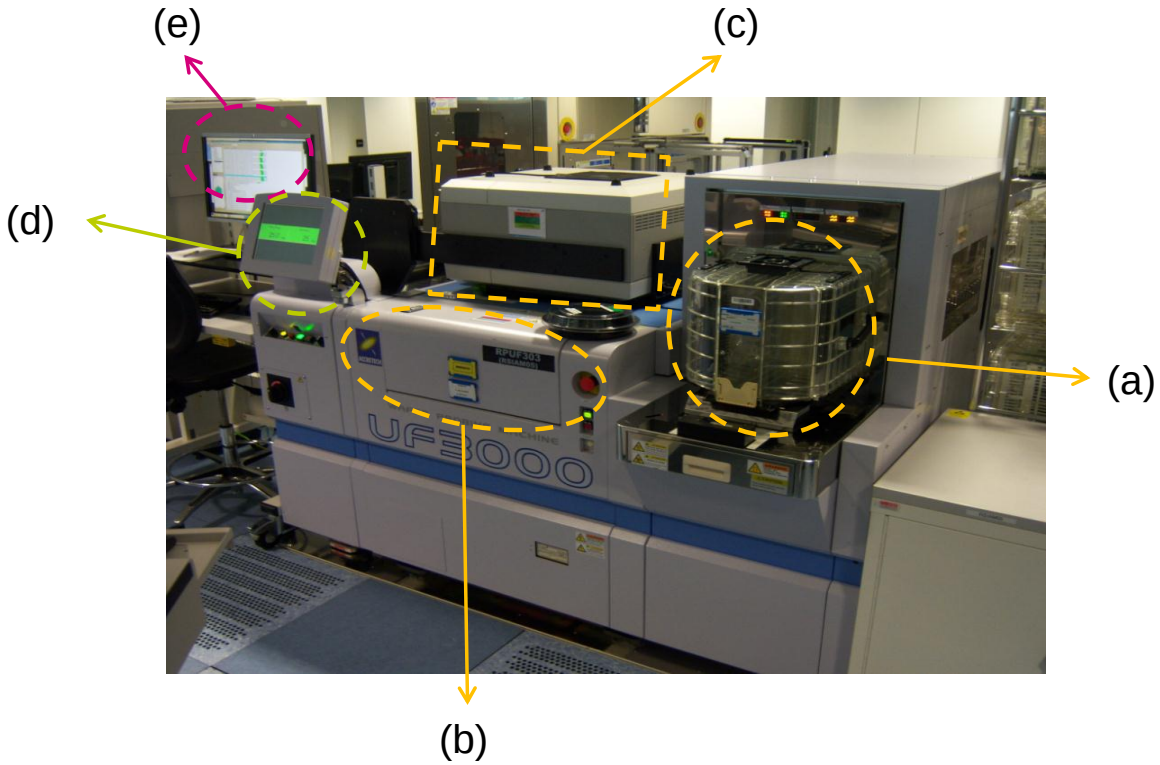


Figure I. 20 : Wafer prober

This equipment consists of:

a- **« FOOP »,** from which the wafers are automatically fed to the prober via a mechanical arm

b- **« Chuck»,** where the wafer to be measured is placed. The chuck can be temperature-controlled and displaced during testing to align the test structure on the wafer with the electrical probes

c- **«Test Head»,** contains the probe card and the switching matrix. The probe card used for mismatch measurements is shown in Figure I. 21.a. It comprises two lines with twelve pins (probes) each and is connected to a switching matrix which connects each pin to the correct SMU (Source/Monitor Unit). A picture of a pin is shown in Figure I. 21.b. Through the SMU, the parameter analyzer supplies the defined voltages/currents and measures the currents/voltages of the devices under test. Finally, before any test,

contact resistance verification is recommended. This test allows validating the contact between the pins and the test structure to prevent any measurement errors. Figure I. 21.c shows a part of resistance test structure not yet tested, while Figure I. 21.d shows a tested part of resistance test structure. Note that this resistance scribe is composed of 24-shorted pads.

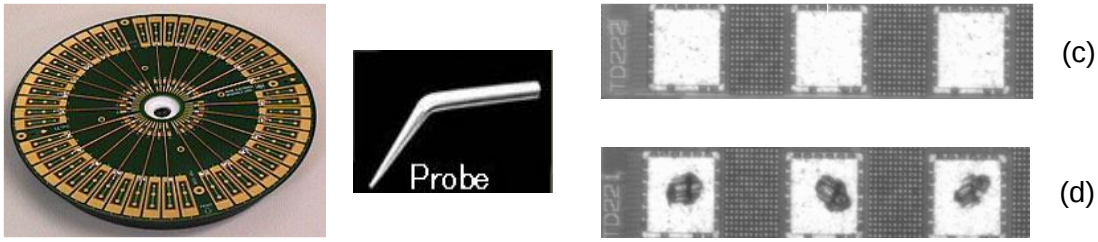


Figure I. 21 : Picture a) a Probe card b) a probe c) not measured scribe d) measured scribe

d- **« Command interface »,** provides the controls to start testing (showing the test structures and the probes).

e- **« Unix station»,** communicates with the measurement equipment and collects the experimental data. It supports programming and test execution via specific software.

I.5.2 Mismatch test structures

The mismatch scribe is shown in Figure I. 22,

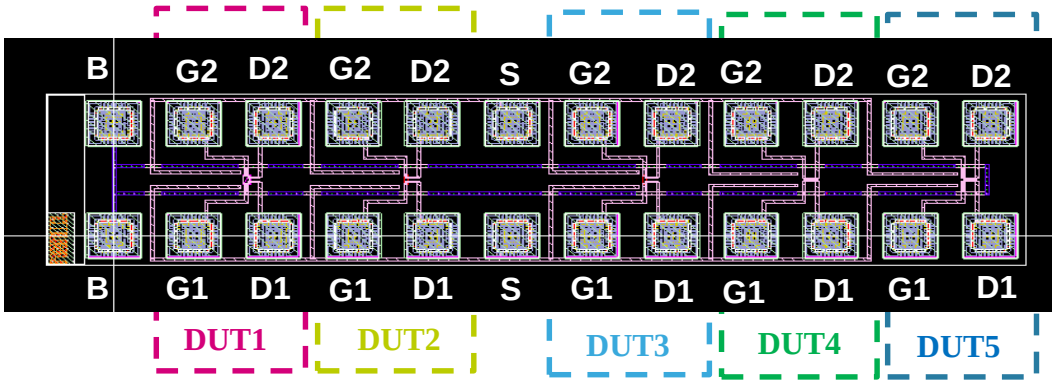


Figure I. 22: Mismatch scribe composed of five pairs of MOS transistors.

This test structure is composed of:

1- 24 pads (2 parallel lines with 12 pads each)

2- 5 pairs of N- or P-type MOS devices of the same technology but different geometries.

3- 2 MOS transistors placed in pairs spaced by the minimum allowed distance, laid out in identical environment and electrically independent with symmetric connections as shown in Figure I. 23. They have common Bulk, separate gate, drain and source and the currents flow through them in the same direction. Gate dummies are also positioned on both sides of transistors gates to improve lithography and etching processes

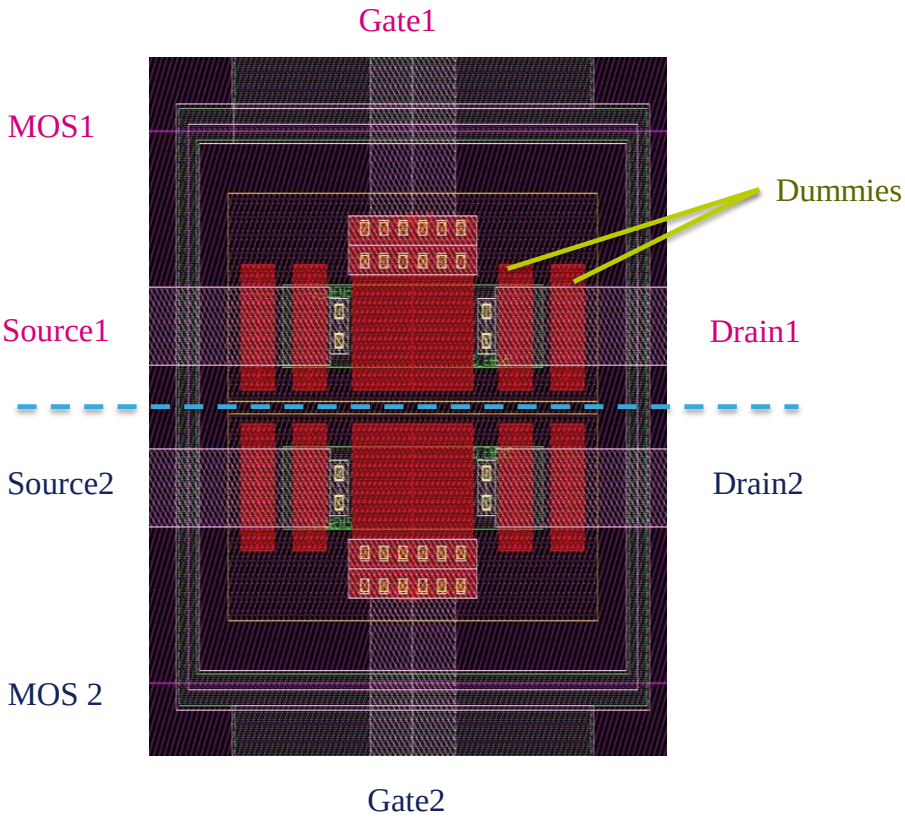


Figure I. 23: MOS transistor pairs (test structure)

4- A protection diode is connected upstream of each gate to prevent the gate oxide from charging during the manufacturing process.

I.6 Stochastic mismatch contributions and effects in Bulk technology: state of the art.

Different studies have been led on the threshold voltage mismatch, demonstrating that the random dopant fluctuations schematically illustrated in Figure I. 24, the poly gate granularity (PGG) in Figure I. 25 and the line edge roughness in Figure I. 26 are the most

important sources of fluctuation in modern bulk MOSFET technologies, up until the 45nm Node [Tuinhout97b], [Difrenza01], [Difrenza02b], [Fukutome06b], [Asenov07] and [Cathignol08b].

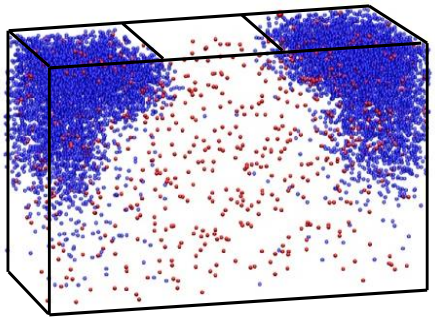


Figure I. 24: Random dopant fluctuation [Asenov00]

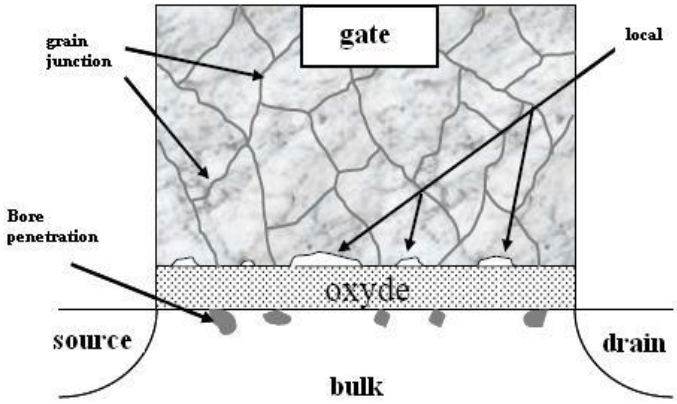


Figure I. 25 : Poly gate granularity [Difrenza03]

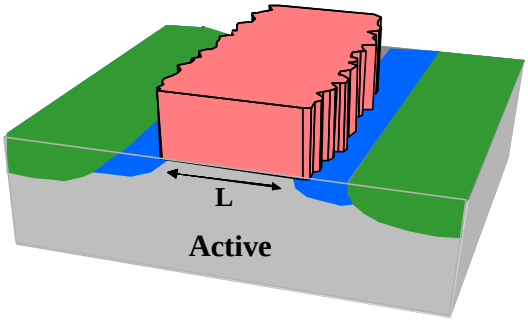


Figure I. 26 : Line edge roughness [Oldiges00]

One of the first studies on the contribution of dopant fluctuations was conducted by Mizuno *et al*. [Mizuno93], [Mizuno94] and [Mizuno96], who experimentally demonstrated that the Vt mismatch follows a Gaussian law that derives from the doping fluctuations in the depletion region of MOS transistors. Their work also shows that the Vt mismatch is directly

proportional to $Nc^{1/4}.Tox$, where *Nc* is the doping concentration and *Tox* the physical oxide thickness.

Since then, and due to the miniaturization of MOS devices, the effects of doping fluctuations on the Vt mismatch have become the main object of various studies [Steyaert94], [Wong 97], [Bastos97] and [Tanaka00]. For short transistors, moreover, short channel effects (SCE) have been observed that are responsible for a reduction in the threshold voltage (Vt). Thus, to enable an ongoing miniaturization of transistor devices, pocket implants were introduced so as to reverse the short channel effects (RSCE) and allow a better modulation of Vt. Pocket implants have been demonstrated to increase the Vt mismatch in short gate transistors, due to the global increase of impurity concentration in the channel [DiFrenza00]. For large gate lengths, instead, the observed mismatch trends do not follow the scaling law any more [Stolk98], [Croon02b] and [Rochereau04]. An exhaustive study of the effects of pocket implants on the Vt mismatch in advanced MOSFET's has finally been presented by Mezzomo *et al.* [Mezzomo10c].

Other studies have been conducted to investigate the effects of polysilicon granularity fluctuations on the Vt mismatch [DiFrenza03], [Cathignol06] and [Brown06], as polysilicon has been the most commonly gate material until the 45nm node. A significant amount of research was also conducted on the investigation of the mismatch effects of Line Edge Roughness (LER) and Gate Width Roughness (GWR) [Oldiges00], [Asenov03], [Xiong04], [Gunther05] and [Fukutome06a]. It has been shown that LER has a more significant contribution in miniaturized transistors, as the roughness of the lithography contours does not scale consistently with the feature size and becomes comparable to the gate length. Finally, an exhaustive study was presented by Cathignol *et al.* [Cathignol08b] that quantifies each mismatch contribution factor for the 45nm technology by assigning percentage values. The study demonstrates that the contribution of random dopant fluctuations (RDF) accounts to 60% of the total observed mismatch.

As for the current gain factor (β) mismatch, DiFrenza showed that the major sources of β variability are the local fluctuations of the number of dopants in the substrate and the interface trap charges at the Si/SiO_2 interface [DiFrenza02a].

Finally, the local fluctuations of the threshold voltage and current gain factor have been shown to be the major sources of the drain current (I_D) mismatch [Lakshmikumar86]. Different models have thus been proposed to explain the behavior of the I_D mismatch, valid in weak inversion region [Forti94], in weak to strong inversion regime as a function of gate bias

and transistor geometry [Croon02a] [Serrano03], and in weak to strong inversion regime and in linear to saturation regime for transistors with pockets [Mezzomo10a]. In advanced technologies such as the 28nm metal gate node, the Rsd contribution was added to the threshold voltage and current gain factor mismatch [Rahhal13], and this term was demonstrated to be a significant contributing factor to the I_D mismatch.

I.7 Improvements due to FD SOI technology

With the reduction of MOS transistors dimensions, different parasitic effects such as the control of SCE appeared limiting the continuous scaling of BULK MOS transistors [Gallon 07]. Different candidates were adopted to replace the BULK technology such as Fin-Shaped Field Effect Transistor (Fin FET, adopted by Intel) [Jan 12] or Silicon On Insulator (SOI) (adopted by STMicroelectronics) [Planes 12], [Arnaud 12]. In this work, SOI transistors have been used and characterized. An illustration of NMOS SOI transistor is shown in Figure I. 27.

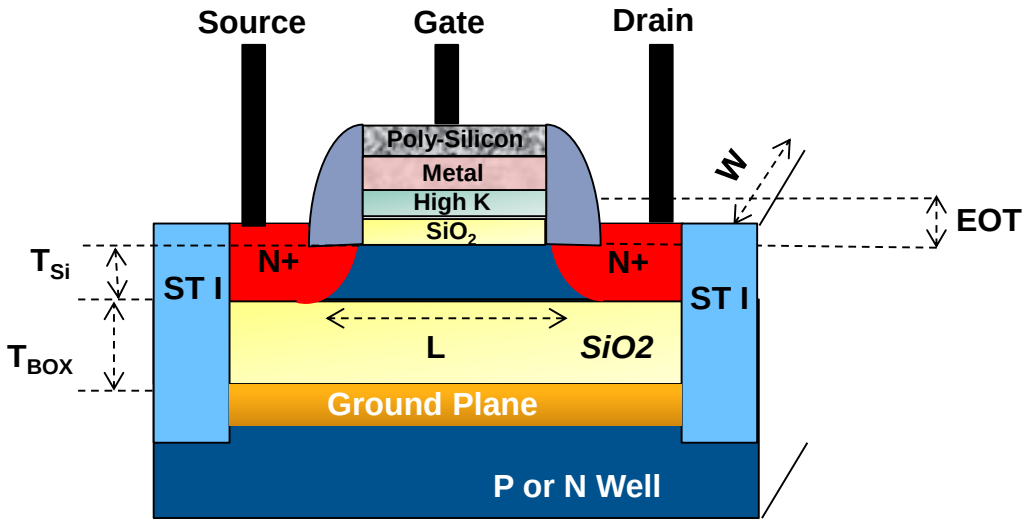


Figure I. 27 : SOI NMOS Transistor

SOI differs from the Bulk technology as transistors are fabricated on an undoped Si layer of thickness T_{Si}. This layer is isolated from the substrate by a buried oxide, called BOX, of thickness T_{BOX}. The active zones are thus defined by the Si Film. Moreover, in some SOI technologies a highly doped zone implanted under the BOX called ground-plane are integrated.

As a consequence two additional features are introduced with respect to Bulk transistors: the undoped Si layer and the BOX.

- If the un-doped Si film is thick enough, then the depletion zone doesn't reach the BOX. In this case the transistor is called partially depleted Silicon On Insulator (PD SOI). The depletion zone T_{dep} is defined in Equation I.30, where Q_{dep} is the depletion charge and N_A the doping concentration.

$$T_{dep} = \frac{Q_{dep}}{q.N_A} \qquad \textbf{(I. 30)}$$

- If a very thin undoped Si film is considered, the depletion zone reaches the BOX and the transistor is called Fully Depleted Silicon On Insulator (FD SOI), as the depletion region spans the whole thickness of the undoped silicon layer.

I.7.1 Main advantages of SOI over BULK technology

FD SOI transistors have many advantages on BULK devices. Many studies have been conducted to characterize, fabricate and demonstrate the benefits of SOI over the BULK technology [Gallon 07], [Barral 07] and [Fenouillet-Beranger 08]. Some of the main advantages of SOI on BULK technology are listed below.

- The use of undoped ultra-thin silicon layer allows a better control of the short channel effects, lower sub-threshold swing, and reduced leakage and Random Dopant Fluctuation (RDF) [Gallon 07].
- FD SOI transistors enable a better electrostatic control because of the shallow source and drain junctions and the thin T_{dep} [Barral 07] and [Fenouillet-Beranger 08].
- The presence of the BOX in FD SOI technology permits a total isolation of the device. Thus, no current circulates in the substrate between devices, preventing latch-up phenomena [Gallon 07].
- The presence of a ground plane enables the threshold voltage to be adjusted via electrostatic coupling through the BOX by setting the doping type and the polarization [Gallon 07]. This coupling gives better electrostatic control compared with bulk devices.
- The reduced depletion region hinders the development of transversal fields and thus improves the carriers' mobility [Gallon 07].

I.7.2 Stochastic mismatch contributions and effects in FD SOI technology: State of the art

FD SOI transistors integrating high k/metal gate and thin BOX exhibit promising characteristics in terms of improved electrical parameters mismatch [Gallon07].

Different studies have been conducted on threshold voltage mismatch, showing that the exclusion of random dopant fluctuations in FD SOI transistors can improve the Vt mismatch and that the metal gate stack is the main contributing factor to the Vt variability [Vinet12]. Vinet *et al*. also showed that other sources of variability (Ground Plane doping, silicon thickness fluctuations) are not recognized as key contributors. Moreover, [Ohtou07] showed that FDSOI transistors with a thin BOX, low channel impurity concentration, and high substrate concentration have high immunity to both process-induced variations and random-dopant-induced variations. This is mainly because the effect of RDFs is suppressed by the impurity charges that are located below the BOX.

Very good matching performance has been reported for advanced FD SOI devices by [Weber08], with a global variability $AVt = 0.95mV.\mu m$. The mismatch value in this case is $iA_{\Delta Vt} = AVt.\sqrt{2}$ [Cathignol 08a]. The authors experimentally distinguish the sources of Vt mismatch in 25nm undoped FDSOI devices integrating a high-k/metal gate stack. Figure I. 28 illustrates the different Vt mismatch contributions. The major contributing factors were identified to be the charges in the gate dielectric and/or the fluctuations of the TiN gate work function. Variations in the undoped silicon thickness (T_{Si}) were found to have a negligible impact until T_{Si}=*7nm*. Finally, the scaling of T_{Si} was shown to limit both local and inter-die Vt variability induced by gate length fluctuations.

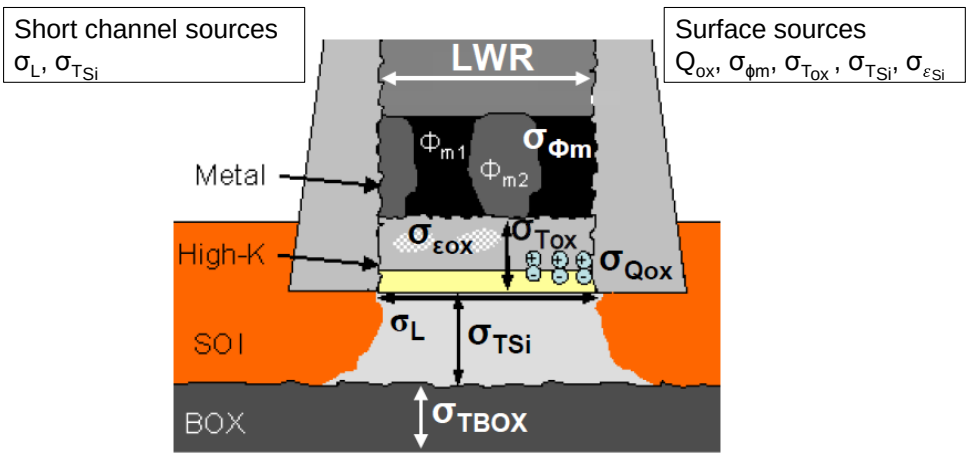


Figure I. 28 : Vt mismatch sources in advanced FD SOI transistors [Weber08]

Atomistic quantification studies were moreover conducted by the Asenov group for advanced FDSOI transistors. The impact of various sources of statistical variability in nominal nano-CMOS transistors was investigated, including random discrete dopants (RDD), line edge roughness (LER), polysilicon granularity (PSG) and oxide thickness fluctuations (OTF) [Asenov07]. The authors also demonstrated that thin BOX in SOI technology can improve the mismatch performance and that SRAMs based on 10 nm ultra-thin BOX perform better than SRAMs based on 35 nm bulk MOSFETs.

Several other positive studies advocating the benefits of FD SOI advanced transistors in terms of reducing threshold voltage have been reported [Sugii10] [Wang12] [Fenouillet-Beranger08]. The influence of silicon thickness on transistor matching has been studied by Hook [Hook11]. The authors showed that device spacing plays a key role in mismatch, that silicon thickness variations depends strongly on the wafer preparation, and that increasing transistor widths can only slightly improve the matching performance, for widths of 1000nm or more. The authors also showed that silicon thickness variations is amenable to improvement through process optimization. One of the process optimization is the use of strained SOI wafers as reported in [Mazurier10].

The presence of the BOX requires studies of the dependence of the statistical variability on the back-gate bias to be also conducted. [Yang13] showed that in the absence of WFV, the application of reverse (negative) back-bias reduces the variability in saturation regime.

Other studies have been reported on the integration of germanium in the channel of ultrathin FDSOI pMOSFETs ($L = 23\ nm$) [Villalon13]. This integration proves to shift the Vt values, yields excellent DIBL and good threshold voltage mismatch performances, with $A\Delta Vt = 1.47 mV.\mu m$.

The mismatch performance in linear and saturation regime has been investigated by [Nauman12]. The authors presented a simple analytical approach to model and characterize the mismatch increase in saturation with respect to the linear mode. The mismatch increase in saturation mode was shown to be mainly due to DIBL variability and induced by RDF in the channel. Hence, the saturated mode mismatch can be reduced by optimizing the channel doping through stronger halo and weaker or counter doped well implants.

Different studies were focused instead on the metal gate granularity (MGG) and on the corresponding work function effects on the threshold voltage variability. [Zhang09] predicted a substantial worsening of the work function variability, inducing comparable or larger threshold voltage mismatch compared with LER and RDF. [Ohmori08], [Dadgour08] and

[Wang11] analyzed in details this new source of variability and attributed it to the metal grain size and orientation.

As for current mismatch, it was demonstrated experimentally in [Mazurier11] that the drain current mismatch is highly correlated with the fluctuations of both Vt and R_{ON}. On the other hand, Markov showed in [Markov12] using atomistic simulations, an enhanced influence of the source/drain dopant fluctuations on the on-current and its mismatch. A comparison between statistical variability in SOI and conventional bulk MOSFETs was proposed in [Hiramoto10]. As for the current mismatch, the authors showed that current-onset voltage variability is well suppressed in the intrinsic channel SOI MOSFETs, thanks to non-intentionally doped channel. Finally [Yang13] demonstrated that the drain current mismatch in saturation is also increased by forward back-biasing of the device. They attributed this increase to the RDF in the source access resistance.

I.8 Conclusions

In this chapter, a general introduction of the MOS transistor conception, modeling and variability was presented and discussed. The state of the art for stochastic mismatch in Bulk technology was subsequently detailed, showing the advantages and the drawbacks of this technology. The FD SOI technology was then introduced as a potential candidate to improve the parasitic effects and the mismatch values and contributions observed in the BULK technology. The FDSOI profile was completed by a detailed state of the art of the associated Stochastic mismatch characteristics. This introduction chapter sets the ground for initial mismatch investigations, analysis and modeling activities on advanced technologies, which are treated in the main part of this thesis.

Chapter II

New method for the extraction of the threshold voltage and current gain factor mismatch and new drain current mismatch model

This methodology chapter proposes a new Y-function based method for the extraction of the threshold voltage (Vt) and current gain factor (β) mismatch. A drain current mismatch model is also proposed that takes into account the value and variability of Rsd.

This chapter is divided into the following five sections.

- Section I discusses the need to revise the drain current mismatch models by considering the influence of the values and variability of Rsd in advanced technologies.
- Section II details a proposed Vt and β mismatch extraction method based on the Y-function statistical variability study. The method is shown to overcome the influence of Rsd values.
- Section III demonstrates a simple drain current mismatch model valid in strong inversion regime that includes the contributions of Vt, β and Rsd values and mismatch.
- Section IV presents the experimental results. The new extraction method and the new drain current mismatch model were applied to 28nm FDSOI and Bulk devices of different dimensions and conclusions are discussed.
- Section V closes the chapter with general conclusions and perspectives.

II.1 Introduction and motivation of this work

The drain current mismatch is one of the critical problems in scaled MOSFET's. Since the beginning of variability studies it has been analyzed that the local fluctuations of the threshold voltage (*Vt*) and current gain factor (β) are the major sources of drain current (I_D) mismatch [Lakshmikumar86] [Croon 02a].

As the channel length is scaled down, the source/drain series resistance (*Rsd*) becomes a non-negligible contribution to the total device resistance (*Rtot*). Figure II. 1.a shows that for long-gate transistors *Rsd* is negligible compared to the channel resistance (*Rch*). However, when the gate length is reduced, *Rsd* is not any more negligible compared to *Rch*, and the total device resistance will be equal to *Rch* + *Rsd* as shown in Figure II. 1.b.

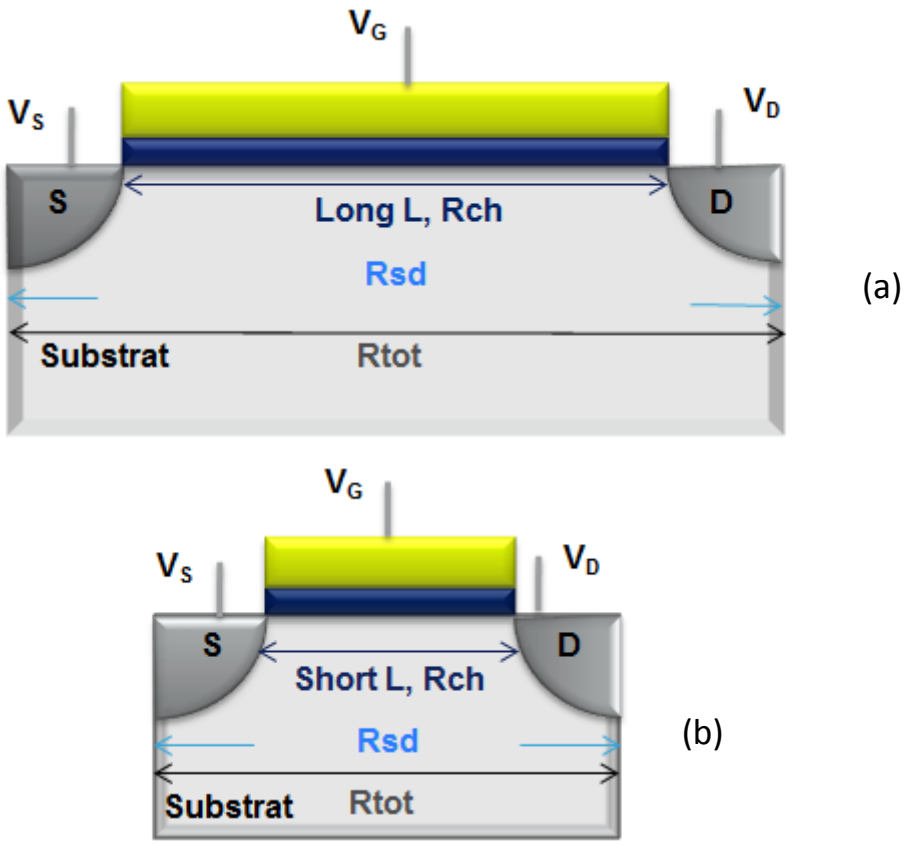


Figure II. 1: BULK MOS transistor (a) with a long gate length (b) with a short gate length

This *Rsd* contribution to the total device resistance has been demonstrated to limit the drain current performance of advanced MOSFET's [Ng 87] & [Thompson 98]. Figure II. 2 shows

that, in strong inversion regime and in the linear region, the drain current decreases when *Rsd* is increased.

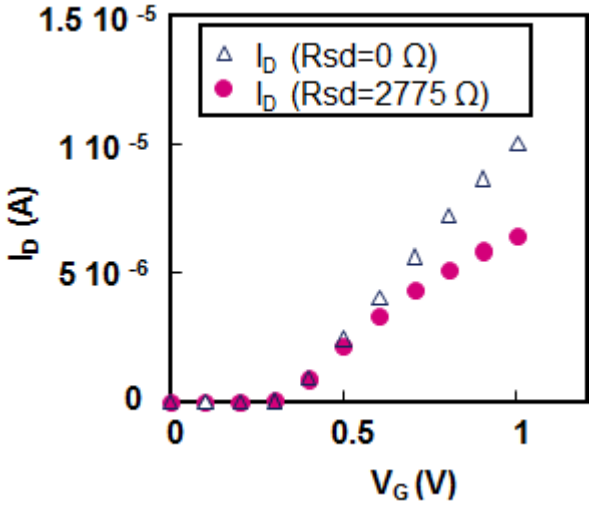


Figure II. 2: Calculation of the drain current values as a function of gate voltage, for Rsd=2775Ω and Rsd=0Ω. (FD SOI transistors with W=0.08µm/L=0.05µm and V_D=50mV)

The plotted curves are obtained using the Equations II.1- II.4 that follow, where *Qi*, Gd_0, *Gd*, *K*, *T*, *n*, and θ_1, θ_2 are respectively the channel inversion charge, the intrinsic channel conductance, the extrinsic channel conductance, the reduced Boltzmann constant, the temperature, the sub-threshold slope ideality factor, and the mobility reduction factors. Typical values are assigned to the parameters to plot the *Rsd* contribution: *L=0.05µm/W=0.08µm* and *Rsd=0* and *Rsd=2775Ω* and drain voltage V_D=*50mV*.

$$Qi = C_{ox}K.T.n.\ln(1+e^{\frac{V_G-V_t}{n.K.T}}).(1-\frac{\ln(1+\ln(1+e^{\frac{V_G-V_t}{n.K.T}}))}{2+\ln(1+e^{\frac{V_G-V_t}{n.K.T}})}) \qquad \textbf{(II. 1)}$$

$$Gd_0 = \frac{\beta}{1+\theta_1.\frac{Q_i}{C_{ox}}+\theta_2.(\frac{Q_i}{C_{ox}})^2}Q_i = C\beta \qquad \textbf{(II. 2)}$$

$$Gd = \frac{Gd_0}{1+Gd_0 Rsd} \qquad \textbf{(II. 3)}$$

$$I_D = Gd.V_D \qquad \textbf{(II. 4)}$$

Moreover, in regards to mismatch issues, Markov showed in [Markov 11] & [Markov 12] that for short channel lengths, the local fluctuations of *Rsd* represent an additional contribution to the drain current mismatch. This phenomenon is more pronounced in ultra-thin silicon body Fully Depleted Silicon On Insulator (FDSOI) devices.

Finally, *Rsd* has an important impact on the I_D values, and its variability has been demonstrated in literature to have an impact on the drain current mismatch. Any future drain current mismatch model for advanced technologies must therefore take into account this contribution.

II.2 New Y-function based mismatch extraction method (strong inversion regime)

The main contributions to the drain current mismatch reported in literature are the threshold voltage and the current gain factor [Lakshmikumar86] [Croon 02a]. Moreover, different techniques and methods to extract the *Vt* and β values have also been reported, as detailed in section I.2.

One of these methods is the Y-function extraction technique, that allows the extraction of the values of *Vt* and β by excluding the Rsd contribution (section I.2.3). In this section a mismatch study was presented where the values of *Vt* and β were extracted for N samples of MOSFET transistor pairs. After applying a recursive filter to eliminate erroneous data, the standard deviation $\sigma_{\Delta Vt}$ and $\sigma_{\Delta\beta/\beta}$ of the Gaussian distribution was calculated (Section I.5).

In this paragraph, however, we propose a direct $\sigma_{\Delta Vt}$ and $\sigma_{\Delta\beta/\beta}$ extraction method, also based on the Y-function extraction technique, that avoids following the previously detailed *Vt* and β extraction steps. As shown in section I.3.3 and Figure II. 3, the Y-function has the advantage to be independent from *Rsd*.

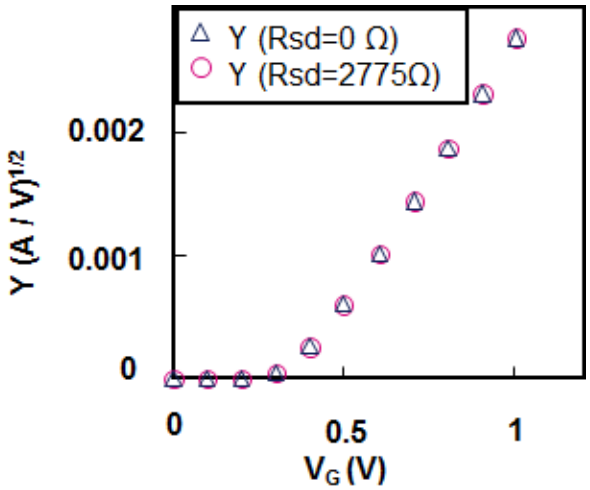


Figure II. 3 : Calculated Y function values as a function of the gate voltage, for Rsd=2775Ω and Rsd=0Ω (FD SOI transistors with W=0.08µm/L=0.05µm and V_D =50mV).

Starting from the Y-function equation (Equation I.15), the Y-function derivative can be written using the first order Taylor approximation, as shown in Equation II.5. In this equation the principal contributions to the variability of the Y function are assumed to be *Vt* and *β*, while the derivative of Y function versus *Rsd* is equal to zero.

$$\frac{dY}{Y} = \left(\frac{1}{Y}\frac{\partial Y}{\partial Vt}\right).dVt + \left(\frac{1}{Y}\frac{\partial Y}{\partial \beta}\right).d\beta \qquad \textbf{(II. 5)}$$

The Y function variance is then calculated as shown in Equation II.6. Note that the correlation between the variability of *Vt* and *β* is deemed negligible.

$$\left(\frac{\sigma_Y}{Y}\right)^2 = \left(\frac{1}{Y}\frac{\partial Y}{\partial Vt}\right)^2.\sigma_{Vt}^2 + \left(\frac{1}{Y}\frac{\partial Y}{\partial \beta}\right)^2.\sigma_{\beta}^2 \qquad \textbf{(II. 6)}$$

If V_G > Vt and V_G falls within a range where θ_2 can be neglected for the calculation of the drain current (Equation I.10 & Equation II.4) and the Y function (Equation I.15), it is possible to write:

$$\frac{\partial Y}{\partial Vt} = \sqrt{\frac{W}{L}\mu_0 Cox V_D} = \sqrt{\beta V_D} \qquad \textbf{(II. 7)}$$

$$\frac{\partial Y}{\partial \beta} = \frac{(V_G - Vt).V_D}{2.\sqrt{\beta.V_D}} \qquad \textbf{(II. 8)}$$

Using Equations I.15, II.6, II.7 and II.8, the Y function variability can be written as shown in Equation II.9.

$$(\frac{\sigma_Y}{Y})^2 = \frac{\sigma_{Vt}^2}{(V_G - Vt)^2} + \frac{1}{4}(\frac{\sigma_\beta}{\beta})^2 \qquad \textbf{(II. 9)}$$

Considering then the difference between two identical MOS devices, the drain current mismatch can be written as shown in Equation II.10. In this equation $\sigma^2_{\Delta Y/Y}(V_G - Vt)^2$ as a function of $(V_G - Vt)^2$ is a linear curve, with intercept with the vertical axis and slope of respectively $\sigma^2_{\Delta Vt}$ and $\frac{1}{4}\sigma^2_{\Delta\beta/\beta}$.

$$\sigma^2_{\Delta Y/Y} = \frac{\sigma^2_{\Delta Vt}}{(V_G - Vt)^2} + \frac{1}{4}\sigma^2_{\Delta\beta/\beta} \qquad \textbf{(II. 10)}$$

To validate Equation II.10, a short channel FD SOI transistor is considered with the parameters below:

a. W=0.08µm/L=0.05µm
b. Vt = 0.34V
c. Tox=15 nm
d. Effective mobility μ_0 = 110cm^2.V^{-1}.s^{-1}, θ_1 =0.3 and θ_1 =0.1
e. Rsd=2775Ω
f. $\partial V_G = \partial Vt$ =0.001V
g. $\partial\beta$ =0.1β
h. $\partial Rsd = 0.1Rsd$
i. $\sigma_{\Delta Vt}$=0.01V, $\sigma_{\Delta\beta/\beta}$ =0.131 and $\sigma_{\Delta Rsd}$ =0.1Rsd

The drain current and Y function mismatch, and Equation II.10 were calculated as a function of $(V_G - Vt)^2$ for V_G values in the range of 0.66 - 1V and for V_D=0.05V. As shown in Figure II. 4, $\sigma^2_{\Delta I_D/I_D}(V_G - Vt)^2$ is not linear as a function of $(V_G - Vt)^2$. Instead,

$\frac{1}{4}\sigma^2_{\Delta\beta/\beta}(V_G - Vt)^2 + \sigma^2_{\Delta Vt}$ is a linear curve and is coincident with the linear curve $\sigma^2_{\Delta Y/Y}(V_G - Vt)^2$. Its intercept with the vertical axis and slope are again respectively $\sigma^2_{\Delta Vt}$ and $\frac{1}{4}\sigma^2_{\Delta\beta/\beta}$.

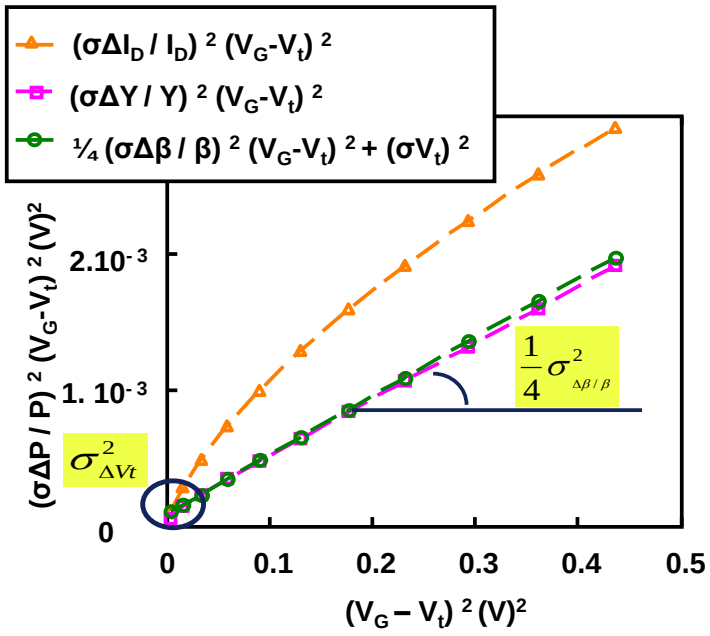


Figure II. 4: Extraction of $\sigma_{\Delta Vt}$ and $\sigma_{\Delta\beta/\beta}$ using $\sigma^2_{\Delta Y/Y}(V_G\text{-}Vt)^2$ as a function of $(V_G\text{-}Vt)^2$ and $\sigma^2_{\Delta ID/ID}(V_G\text{-}Vt)^2$ as a function of $(V_G\text{-}Vt)^2$ (FD SOI transistors with W=0.08µm/L=0.05µm and V_D =50mV , Vt=0.34V).

The benefit of this new extraction method lies in its easy and rapid application, and in its independence from the values and variability of Rsd. The classical Y-function extraction method requires the extraction of *Vt* and *β*, followed by the calculation of their mismatch. However, the new Y function mismatch extraction technique proposed in this paragraph (equation II.10) enables a direct extraction of *Vt* and *β* mismatches by simply considering the standard deviation of the Y function in strong inversion regime. Note that to maintain robustness with respect to the θ_2 parameter while using this method, V_G should not be very high (V_{Gmax} = 1V for this study).

II.3 New drain current mismatch model

Different models have been proposed to explain the behavior of I_D mismatch: in weak inversion region [Forti 94], in weak to strong inversion regime as a function of gate bias and transistor geometry [Serrano 03], and in weak to strong inversion regime and in linear to saturation regime for transistors with pockets [Mezzomo 10a]. A mismatch model has been published by Croon [Croon 02a] that expresses the drain current mismatch as a function of the threshold voltage and current gain factor mismatch, the surface roughness scattering and the saturation velocity. This model gives mismatch trends as a function of the gate bias and of transistor geometries.

As shown in section II.1, Rsd has an important impact on I_D. We therefore propose a new drain current mismatch model that takes into account the influence and variability of Rsd.

Starting from the first order Taylor approximation of the drain current, the principal contributions to I_D variability are, based on literature, Vt, β and Rsd. The drain current derivative can be written as shown in Equation II.11.

$$\frac{dI_D}{I_D} = \left(\frac{1}{I_D}\frac{\partial I_D}{\partial Vt}\right).dVt + \left(\frac{1}{I_D}\frac{\partial I_D}{\partial \beta}\right).d\beta + \left(\frac{1}{I_D}\frac{\partial I_D}{\partial Rsd}\right).dRsd \qquad \textbf{(II. 11)}$$

Calculating the drain current variance, the drain current variability can be written as shown in Equation II.12. Note that the cross-correlations factors between the Vt, β and Rsd variabilities are considered negligible.

$$\left(\frac{\sigma_{I_D}}{I_D}\right)^2 = \left(\frac{1}{I_D}\frac{\partial I_D}{\partial Vt}\right)^2.\sigma_{Vt}^2 + \left(\frac{1}{I_D}\frac{\partial I_D}{\partial \beta}\right)^2.\sigma_{\beta}^2 + \left(\frac{1}{I_D}\frac{\partial I_D}{\partial Rsd}\right)^2.\sigma_{Rsd}^2 \qquad \textbf{(II. 12)}$$

If $V_G > Vt$ and V_G is in a range where θ_2 can be neglected for the calculation of the drain current (Equation I.10 & Equation II.4), the partial derivatives of I_D using Equations I.10 and II.4 are calculated with respect to Vt, β and Rsd in Equations II.13, II.14, II.15, II.16 and II.17. The drain current variability model is thus obtained in Equation II.18, where Gm is the trans-conductance.

$$\frac{\partial I_D}{\partial Vt} = \frac{\beta V_D\left[1+\theta_1(V_G-Vt)\right]+\theta_1\left[\beta V_D(V_G-Vt)\right]}{\left[1+\theta(V_G-Vt)\right]^2} = \frac{\beta V_D}{\left[1+\theta(V_G-Vt)\right]^2} = Gm \qquad \textbf{(II. 13)}$$

$$\frac{\partial I_D}{\partial \beta} = \frac{C(1+C\beta Rsd - C^2\beta.Rsd).V_D}{(1+C\beta.Rsd)^2} = \frac{C}{(1+C\beta.Rsd)^2}V_D \qquad \textbf{(II. 14)}$$

$$\frac{1}{I_D}.\frac{\partial I_D}{\partial \beta} = \frac{1}{\beta.(1+C\beta.Rsd)}.\frac{C\beta}{C\beta} = \frac{1}{\beta}.\frac{Gd}{Gd_0} \qquad \textbf{(II. 15)}$$

$$Gd + Gd.Gd_0Rsd = Gd_0 \Rightarrow \frac{Gd}{Gd_0} = 1 - GdRsd \qquad \textbf{(II. 16)}$$

$$\frac{\partial I_D}{\partial Rsd} = -\frac{Gd_0^2.V_D}{(1+Gd_0Rsd)^2} = -Gd^2.V_D = -I_D.Gd \qquad \textbf{(II. 17)}$$

$$\left(\frac{\sigma_{I_D}}{I_D}\right)^2 = \left(\frac{Gm}{I_D}\right)^2.\sigma_{Vt}^2 + (1-Gd.Rsd)^2.\left(\frac{\sigma_\beta}{\beta}\right)^2 + (Gd)^2.\sigma_{Rsd}^2 \qquad \textbf{(II. 18)}$$

For mismatch studies, considering the difference between two identical MOS transistors, Equation II.18 can be written as shown in Equation II.19 that represents the new drain current mismatch model

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{Gm}{I_D}\right)^2.\sigma^2_{\Delta Vt} + (1-Gd.Rsd)^2.\sigma^2_{\Delta\beta/\beta} + (Gd)^2.\sigma^2_{\Delta Rsd} \qquad \textbf{(II. 19)}$$

II.3.1 Validation of the new drain current mismatch model

In order to validate the new drain current mismatch model in Equation II.19, the same short channel FD SOI transistor as section II.2 is considered with W=0.08µm and L =0.05µm. The three models below are plotted as a function of V_G in Figure II. 5:

a- Theoretical drain current mismatch represented by Equation II.12. Note that in Equation II.12 the difference between two identical MOS devices are used: $\sigma_{\Delta Vt}$=0.01V, $\sigma_{\Delta\beta/\beta}$ =0.131 and $\sigma_{\Delta Rsd}$ =0.1Rsd

b- Drain current mismatch model represented by Equation II.19

c- Croon's model [Croon 02a] expressed in Equation II.20 (where Vt-β correlation, surface roughness scattering and saturation velocity have been neglected).

Note that Vt and β standard deviations are extracted using the new Y function mismatch extraction method proposed in section II.2.

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{Gm}{I_D}\right)^2 .\sigma^2_{\Delta Vt} + \sigma^2_{\Delta\beta/\beta} \qquad \textit{(II. 20)}$$

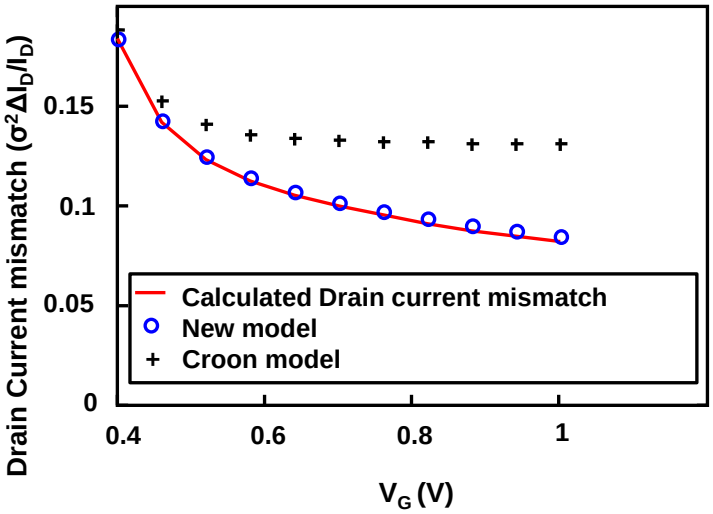


Figure II. 5: Comparison between calculated full drain current mismatch, drain current mismatch model and Croon model without correlation, roughness scattering and saturation velocity terms (FD SOI transistors with W=0.08µm/L=0.05µm and V_D =50mV).

Figure II. 5 shows that, Croon's model does not reproduce the calculated drain current mismatch for short gate length (L=0.05µm). It is moreover possible to improve Croon's model by multiplying $\sigma^2_{\Delta\beta/\beta}$ by $(1-Gd.Rsd)^2$ (which represent the Rsd contribution and thus the mobility attenuation) and by excluding the Vt-β correlation term, so that the theoretical drain current mismatch is reproduced.

II.4 Experimental Results

II.4.1 Experimental setup

Electrical characterizations have been carried out on 28 nm FD-SOI and Bulk devices integrating High-k gate oxide and metal gate. A sample of 70 pairs of identical MOS transistors has been considered, with the test structures detailed in section I.5.2. All presented results refer to measurements performed in linear regime with drain voltage V_D=50mV and gate voltage ranging from 0 to 1V, at 25°C.

II.4.2 FD SOI NMOS transistors of moderate gate length (W=1µm/L=0.1µm)

Starting from NMOS transistors of moderate length (L=0.1µm), the drain current I_D is measured and plotted in Figure II. 6 as a function of V_G. The Y function is calculated from the drain current using Equation I.15 and plotted in Figure II. 7 as a function of V_G. Figure II. 6 & Figure II. 7 show typical behaviors of I_D and Y as a function of V_G.

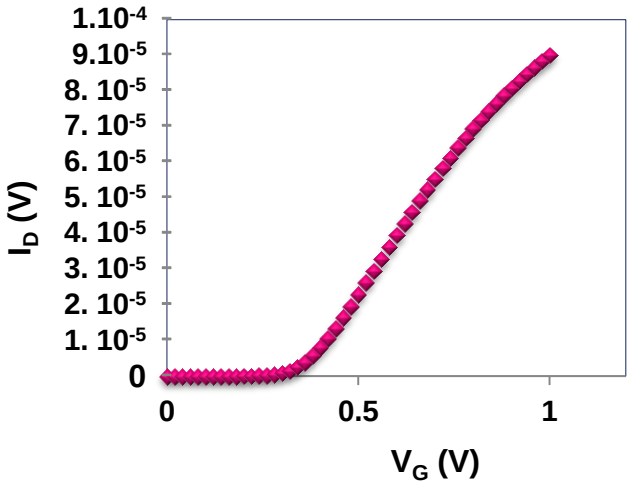


Figure II. 6: Drain current as a function of gate voltage (FD SOI transistors with W=1µm/L=0.1µm and V_D =50mV).

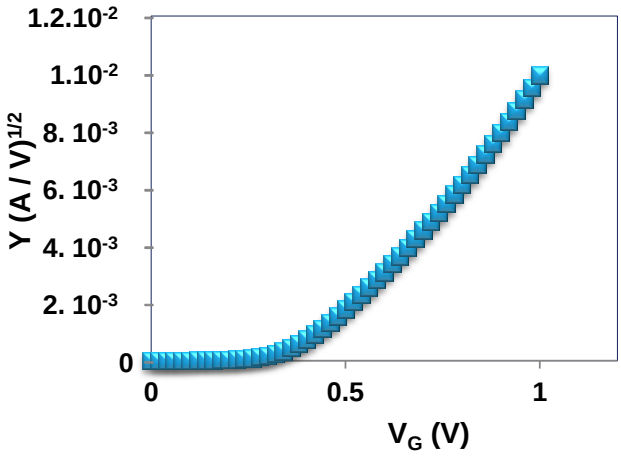


Figure II. 7: Y Function as a function of gate voltage (FD SOI transistors with W=1µm/L=0.1µm and V_D =50mV).

The relative difference of I_D (noted $\Delta I_D/I_D$) and Y (noted $\Delta Y/Y$) between the pair of MOS transistors are calculated. This method is repeated for 70 pairs of identical NMOS transistors. The standard deviations of $\Delta I_D/I_D$ and $\Delta Y/Y$ are then calculated. Subsequently, the quantities $\sigma^2_{\Delta I_D/I_D}.(V_G - Vt)^2$ and $\sigma^2_{\Delta Y/Y}.(V_G - Vt)^2$ are plotted as a function of $(V_G - Vt)^2$ in Figure II. 8. This graph shows that while $\sigma^2_{\Delta I_D/I_D}(V_G - Vt)^2$ as a function of $(V_G - Vt)^2$ might be nonlinear due to the combined effect of Rsd and mobility degradation, $\sigma^2_{\Delta Y/Y}(V_G - Vt)^2$ presents a better linearity as a function of $(V_G - Vt)^2$, with a correlation of 0.98. Using Equation II.10, $\sigma^2_{\Delta Vt}$ and $\sigma^2_{\Delta\beta/\beta}$ are finally extracted with a method that excludes the influence of Rsd.

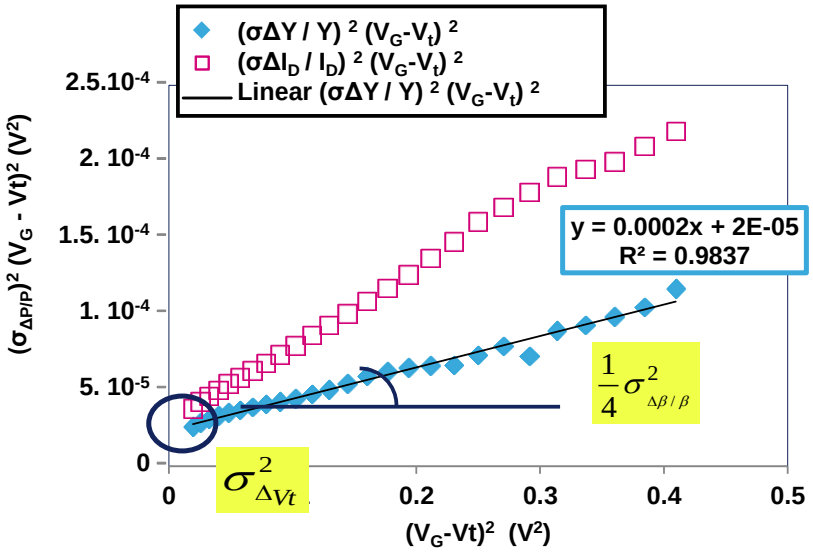


Figure II. 8: V_G>V_t (V_G in the range of 0.6 -1V, with Vt=0.36V), Y function and drain current mismatch multiplied by $(V_G\text{-}Vt)^2$ and plotted as a function of $(V_G\text{-}Vt)^2$ (FD SOI transistors with W=1µm/L=0.1µm and V_D =50mV).

To verify if the values of Vt and β mismatch are correct, $\sigma^2_{\Delta Vt}$ and $\sigma^2_{\Delta\beta/\beta}$ are extracted using the classical Y function method explained in section I.2.3. Table II.1 represents a comparison between $\sigma^2_{\Delta Vt}$ and $\sigma^2_{\Delta\beta/\beta}$ extracted with the classical Y function method and the new Y Function method. It does not show significant difference between the two methods.

Table II.1: Comparison between Vt and β mismatch extracted by classical and new Y function extraction methods.

$(\sigma Parameter)^2$	$(\sigma_{\Delta Vt})^2$	$(\sigma_{\Delta\beta/\beta})^2$
Mismatch values extracted with the classical Y function method	$3.10^{-5}\,V^2$	9.10^{-4}
Mismatch values extracted with the new mismatch extraction method ($\sigma^2_{\Delta Y/Y}$)	$2.10^{-5}\,V^2$	8.10^{-4}

In order to validate the new mismatch model proposed in experimentally Equation II.19, first, the values of $\sigma^2_{\Delta Vt}$ and $\sigma^2_{\Delta\beta/\beta}$ are extracted using the new Y function mismatch method. Second, the values of Rsd are extracted using the $R_{tot}=f(1/\beta)$ method proposed by [Fleury 09]. The Rsd extraction technique is shown in Figure II. 9 where Rsd is the intercept of Rtot (1/β) on the vertical axis. This figure shows that the extracted value $Rsd=216.84\Omega$ is not negligible for short devices, where Rtot falls in the range of 300 Ω - 500 Ω for gate lengths ranging between 0.03 and 0.06 µm.

The new drain current mismatch model is then calculated with Equation II.19 using the obtained values for $\sigma^2_{\Delta Vt}$, $\sigma^2_{\Delta\beta/\beta}$ and Rsd. Note that the $(Gd)^2.\sigma^2_{\Delta Rsd}$ term in Equation II.19 can be neglected due to the moderate gate length [Markov 11] & [Markov 12]. The measured drain current mismatch, Croon's model [Croon 02a] expressed by Equation II.20 (without Vt-β correlation) and the new drain current mismatch model are plotted as a function of V_G in Figure II. 10 for the strong inversion regime.

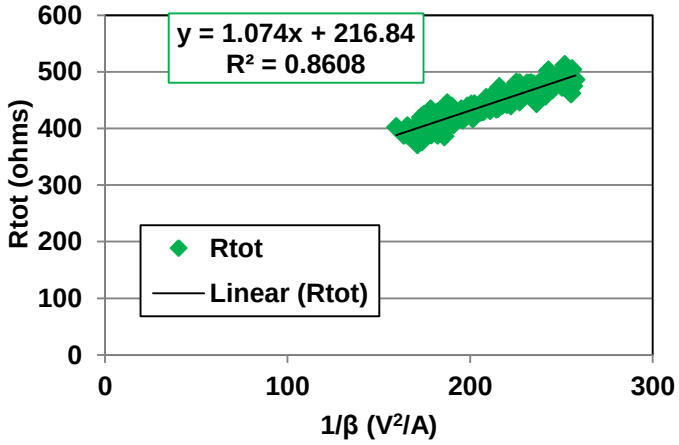


Figure II. 9 Rsd extraction using the $R_{tot}=f(1/\beta)$ method for W=1µm and L=0.03µm, 0.05µm, 0.06µm, and 0.1µm, for NMOS FD SOI transistors with V_G=1V and V_D=50mV.

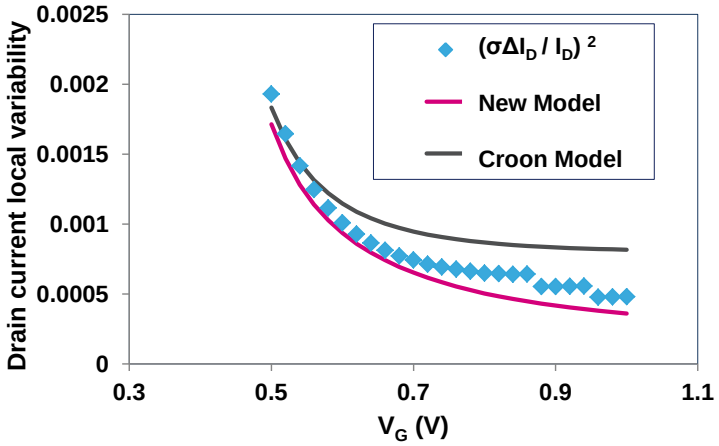


Figure II. 10: V_G>Vt (V_G in the range of 0.5-1V, with Vt=0.36V). Comparison between the new drain current mismatch model, the drain current mismatch model proposed by Croon and the measured drain current mismatch as a function of V_G (FD SOI transistors with W=1µm/L=0.1µm and V_D =50mV, Rsd=220Ω).

Figure II. 10 shows that Croon's model without the Vt-β correlation term does not fit the measured data. Thus, after improving Croon's model, by multiplying $\sigma^2_{\Delta\beta/\beta}$ by $(1-Gd.Rsd)^2$ (which represent the Rsd contribution), the drain current mismatch is well reproduced without any need for Vt-β correlation, indicating also that the Rsd variability is negligible. The interest of this new model is that, while [Croon 02a] must use Vt-β correlation term to fit the data, the new drain current variability model well accounts for the measured data only by considering the Rsd contribution.

II.4.3 FD SOI NMOS transistors with short gate length (W=0.08µm/L=0.05µm)

In this paragraph, the same approach as section II.4.2 is considered for short gate lengths. For each pair of MOS transistors, I_D and Gm are first measured, and then the Y function is calculated from I_D using Equation I.15. The standard deviations of $\Delta I_D/I_D$ and $\Delta Y/Y$ are then calculated for 70 pairs of identical NMOS transistors. Subsequently, the quantities $\sigma^2_{\Delta I_D/I_D}.(V_G-Vt)^2$ and $\sigma^2_{\Delta Y/Y}.(V_G-Vt)^2$ are plotted as a function of $(V_G-Vt)^2$ in Figure II. 11. This figure shows again that, while $\sigma^2_{\Delta I_D/I_D}(V_G-Vt)^2$ as a function of $(V_G-Vt)^2$ might be nonlinear, $\sigma^2_{\Delta Y/Y}(V_G-Vt)^2$ presents a better linearity as a function of $(V_G-Vt)^2$.

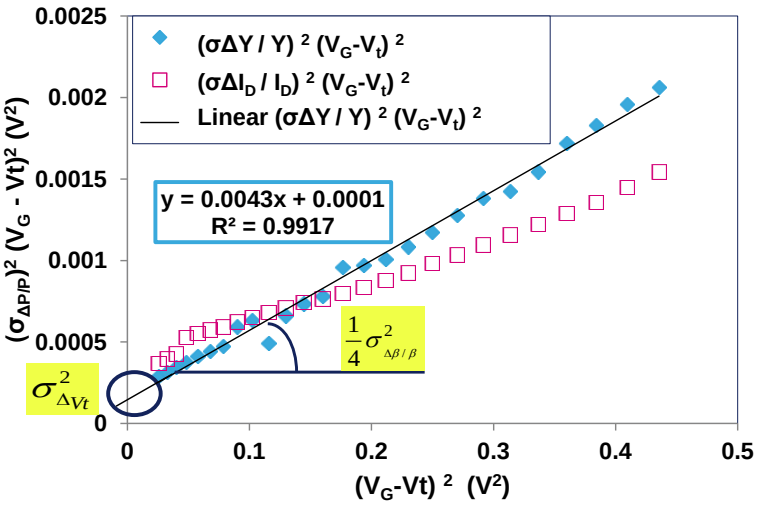


Figure II. 11: V_G>Vt (V_G in the range of 0.5-1V, with Vt=0.34V). Y function and drain current mismatch multiplied by $(V_G-Vt)^2$ and plotted as a function of $(V_G-Vt)^2$ (FD SOI transistors with W=0.08µm/L=0.05µm and V_D =50mV).

Using Equation II.10, $\sigma^2_{\Delta Vt}$ and $\sigma^2_{\Delta\beta/\beta}$ are then calculated, yielding $\sigma^2_{\Delta Vt}=10^{-4}V^2$ and $\sigma^2_{\Delta\beta/\beta}=0.0172$.

Once values have been obtained for $\sigma^2_{\Delta Vt}$ and $\sigma^2_{\Delta\beta/\beta}$, the new drain current mismatch model of Equation II.19 is calculated with the Rsd value extracted using the $R_{tot}=f(1/\beta)$ method shown in [Fleury 09]. Note that at the first order the $(Gd)^2.\sigma^2_{\Delta Rsd}$ term in Equation II.19 is negligible. The measured drain current mismatch, Croon's model [Croon 02a] (without correlation) expressed by Equation II.20, and the new drain current mismatch model are plotted as a function of V_G in Figure II. 12.

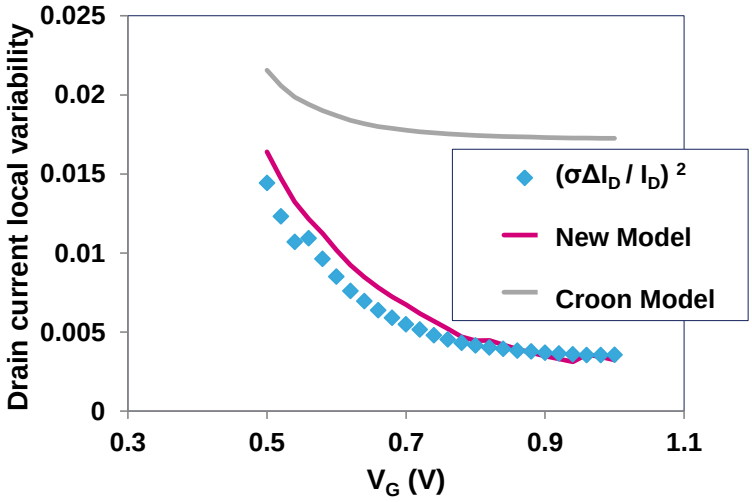


Figure II. 12: V_G>Vt (V_G in the range of 0.5-1V, with Vt=0.34V). Comparison between the new drain current mismatch model, Croon's drain current mismatch model and the measured drain current mismatch as a function of V_G (FD SOI transistors with W=0.08µm/L=0.05µm and V_D =50mV, Rsd=2775Ω).

Figure II. 12 shows that, for short lengths, Croon's model without the Vt-β correlation term also does not fit the measured data. Conversely, by improving Croon's model as in Equation II.19, the new drain current mismatch model enables the experimental variability data to be very well reproduced. Note that the Rsd variability is negligible also in the case of short lengths. Another observation is that the gap between Croon's model (without Vt-β correlation) and the new drain current variability model is more prominent for L=0.05µm than for L=0.1µm. Thus, Rsd value and β mismatch have more impact on I_D mismatch for short lengths, emphasizing the benefit of the new drain current variability model.

II.4.4 Bulk NMOS transistors with short gate length (W=10µm/L=0.03µm)

The new Vt and β mismatch extraction method has also been applied with success to bulk NMOS devices (W=10µm/L=0.03µm, V_D=50mV) as illustrated in Figure II. 13, where $\sigma^2_{\Delta Vt} = 3.10^{-5} V^2$ and $\sigma^2_{\Delta\beta/\beta} = 4.10^{-4}$.

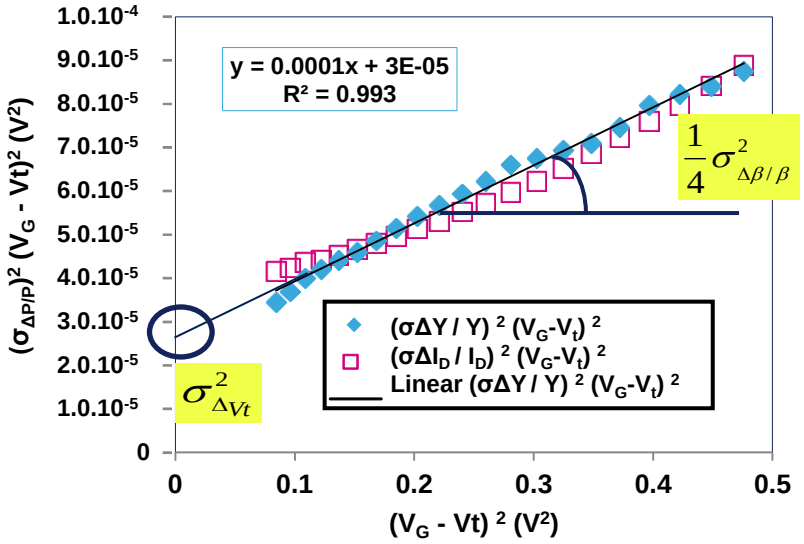


Figure II. 13: V_G>Vt (V_G in the range of 0.6-1V, with Vt=0.31V). Y function and drain current mismatch multiplied by $(V_G\text{-}Vt)^2$ and plotted as a function of $(V_G\text{-}Vt)^2$ (BULK transistors with W=10µm/L=0.03µm and V_D =50mV).

Once values for $\sigma^2_{\Delta Vt}$ and $\sigma^2_{\Delta\beta/\beta}$ have been obtained, and once Rsd is extracted using [Fleury 09], the new drain current mismatch model of Equation II.19 was also applied with success to this measurement data. Figure II. 14 shows that, using the new drain current mismatch model, the measurement drain current mismatch data are well reproduced in strong inversion regime.

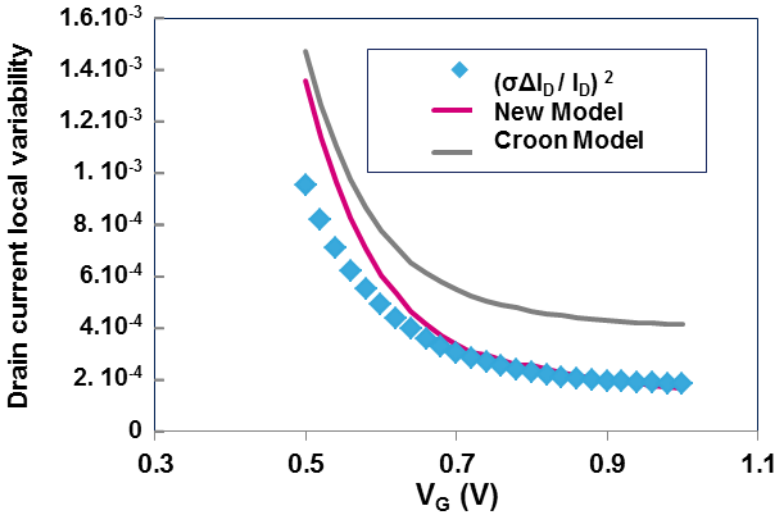


Figure II. 14: V_G>Vt (V_G in the range of 0.5-1V, with Vt=0.31V). Comparison between the new drain current mismatch model, Croon's drain current mismatch model and the measured drain current mismatch as a function of V_G (Bulk transistors with W=1µm/L=0.03µm and V_D =50mV, Rsd=23Ω).

II.5 Conclusions

After showing the impact of Rsd on the drain current in short devices, a new threshold voltage and current gain factor mismatch method was demonstrated. This method excludes the influence of Rsd and is based on the well-known Y function. Also, a new drain current mismatch model based on the values and variability of Vt, β and Rsd valid in strong inversion regime was demonstrated. The new extraction method and the new drain current mismatch model were successfully applied to measured data for 28 nm FD SOI and Bulk NMOS transistors of different lengths and widths.

For future technologies, this model can also be used to extract the contribution of the variability of Rsd to the variability of the drain current. Note that in the case of 28nm Bulk and FD SOI technology this variability was demonstrated to be negligible. Note that by considering Vt-β correlation term in Croon and Improved Croon Model, this correlation is demonstrated to be negligible in all devices characterized in this thesis (Appendix A).

Chapter III

Cascode configuration as a substitute to LDE MOSFET for improved electrical mismatch performance

The work presented in this chapter aims at optimising the mismatch performances of circuit configurations based on design considerations. In light of this, the option of replacing a Lateral Drain Extended MOS (LDEMOS) SOI transistor by a cascode configuration with the aim of improving the electrical mismatch performance is investigated. The cascode connection of two MOS devices is known to sustain as high drain voltage as LDEMOS SOI transistors. The investigation herein detailed aims at discovering whether this configuration offers the same mismatch robustness as Silicon On Insulator (SOI) MOS transistors.

This chapter is divided into the following four sections:

- Section I is a general introduction of the three devices considered for this study, with a particular focus on their advantages and drawbacks in terms of sustaining high drain voltages, mismatch issues and contributing factors.
- Section II provides details on the measurement conditions and test structures.
- Section III is divided in two parts. The mismatch behaviour of Vt, β and I_D for the three devices is discussed for linear regime in part I and for saturation regime in part II.
- Section IV draws general conclusions and proposes perspectives for future work.

III.1 Introduction and motivation of this work

In the field of power management, some analogue applications (current mirrors, power amplifiers…) require matched pair of MOS transistors that can sustain high drain voltages. It is thus crucial to select MOS transistor types and architectures that combine adequate mismatch performance and the ability to sustain high voltages.

Usually the classical MOS transistor is considered. In this study a partially depleted SOI, P type transistor is considered as illustrated in Figure III. 1. This device of L=0.28µm/W=0.7µm has a floating body and an oxide thickness of 5nm. It also has a good channel length control with L_channel ≈ L_gate. Little variability is thus introduced by the channel length. This device shown in Figure III. 1cannot however individually sustain high drain voltages.

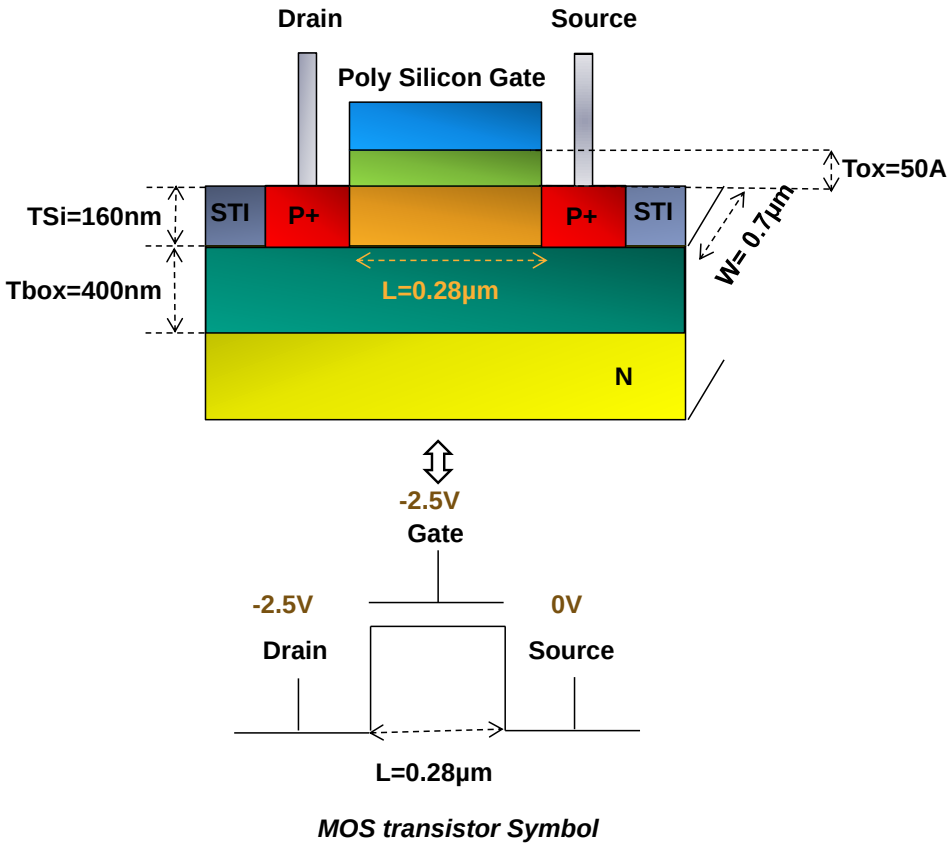


Figure III. 1: Partially depleted SOI PMOS transistor with thick oxide (Tox=5nm) with L=0.28µm and W=0.7µm.

Multiple architectures exist for high voltage (HV) devices, which can be selected based on the desired trade-off such as, for instance, (Ron.Surface), breakdown, reliability or fabrication cost. Among the different available architectures, the Lateral Drain Extended MOS (LDEMOS) on Silicon On Insulator (SOI) transistor shown in Figure III. 2 is of particular interest. This device is known to sustain high drain voltages [Ishikawa 85], [Kim 00] and [D'Halleweyn 04] due to its extended resistance between the drain and the channel. In Figure III. 2, a partially depleted SOI, P type transistor with multi-fingered structure is considered. However, due to the diffused channel where L_gate=0.4µm ≠ L_channel=0.25µm, the gate length is not well controlled, thus introducing a significant source of variability.

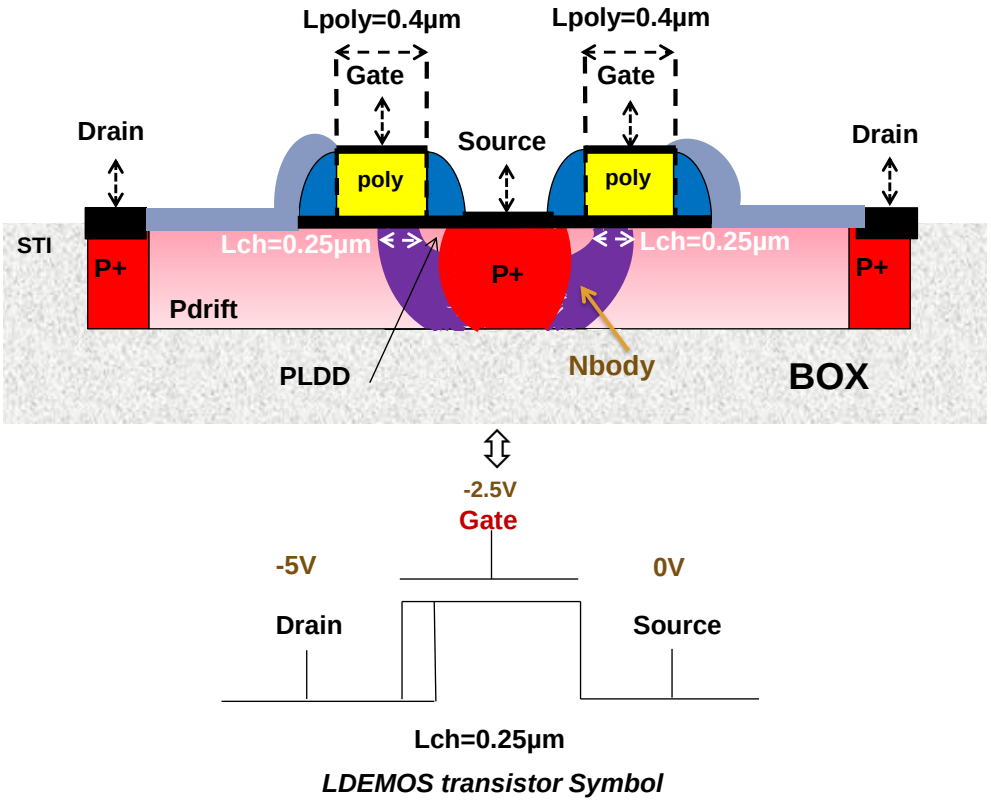


Figure III. 2: PLDE MOS, The device is fabricated on SOI, with a polysilicon gate length of 0.4µm, gate oxide thickness of 5nm, Box thickness (tbox) of 400nm, SOI thickness (tSi) of 160nm and an estimated channel length of 0.25µm.

Another potential solution for devices that can sustain high drain voltages is the cascode connection two or more MOSFET's illustrated in Figure III. 3. In this figure two MOS devices connected in cascode configuration are considered, with the aim of combining the

mismatch properties of MOS devices with the ability to sustain high drain voltages of LDEMOS. The source of the first MOS (MOS1) is connected to the drain of the second MOS (MOS2) to form a floating node. The drain of MOS1 is then considered as the drain of the overall device, while the source of MOS2 is considered as the source of the overall device. Note that this device presents two separate gates. This configuration offers the advantage of being able to sustain high drain voltages up to 5V. The challenge, however, is to maintain the same mismatch values as those observed in individual MOSFET.

The purpose of this work is to examine the mismatch performance of this specific architecture as compared to the well-known individual and LDEMOS devices.

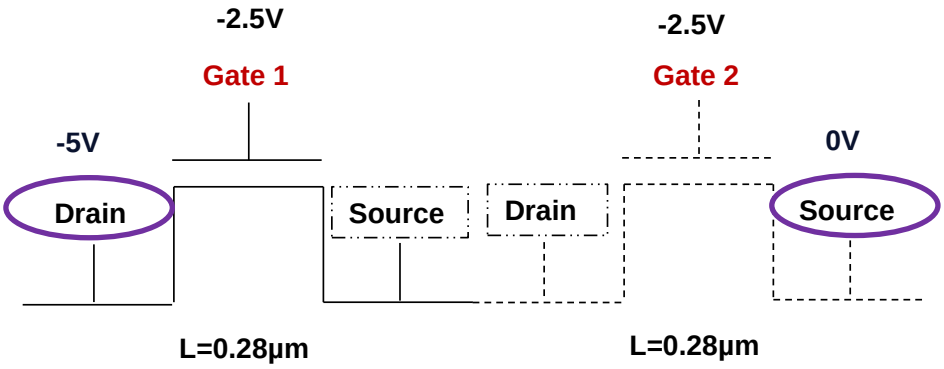


Figure III. 3 Two cascode-connected PMOS devices with L1=L2=0.28µm and W=0.7µm

III.2 Experimental details

Electrical characterisation was performed on partially depleted silicon on insulator (PD-SOI) PMOS transistors of different types, such as LDEMOS, individual MOSFET and MOSFET connected in cascode configuration. The oxide thickness is Tox=5nm, constant for all the devices under test. For matching measurements, a sample of 136 pairs of identical MOS transistors was considered within the mismatch test structures of Section I.5.2. All the presented results refer to measurements performed at 25°C.

In this work the individual mismatch constant of Equation I.29 is considered. This parameter allows the evaluation of the mismatch values for each channel dimension (Section I.4.5.c).

III.3 Vt, β and I_D mismatches comparison for LDEMOS, Individual and cascode configuration devices.

The high drain voltage matched pair of MOS transistors can be used for analogue applications in linear and saturation regimes. In this section the electrical parameters of the three devices types are characterised and analysed in linear and saturation regimes.

III.3.1 Linear Regime

In linear regime, Vt, β and I_D were measured at V_G=-2.5V and V_D=-0.1V for all devices. As a first order approximation, the total gate length in the cascode configuration was assumed to be the sum of the gate lengths of the two connected devices.

III.3.1.a Vt and β mismatch

The $I_D(V_G)$ characteristics were first measured for all devices of the same width W=10µm and specific lengths L (L=0.25µm for LDEMOS device, L=0.28µm for individual MOS devices and L1=L2=0.28µm for the cascode configuration). The curves reported in Figure III. 4 show that at maximum $|V_G|$, LDEMOS and cascode devices have identical performance, while the individual MOS device exhibits almost double I_D values. Moreover, individual and cascode configuration devices conduct the same I_{Doff} current, while LDEMOS devices exhibit an improved characteristic with lower off current. Note that the cascode configuration has a gate length value which is double than that of individual MOS devices, hence the I_D value at max V_G is almost halved.

The threshold voltage was measured for all devices using the maximum slope method proposed by Hao *et al*. [Hao 85] and the absolute values were plotted as a function of the area S of the MOS transistors. The obtained graph is reported in Figure III. 5. Note that all LDEMOS devices have same gate length (L=0.4µm), same channel length (0.25µm) and different gate widths and number of fingers. The channel length value has been extracted based on capacitance measurements using the method proposed by Valtonen *et al*. [Valtonen 01].

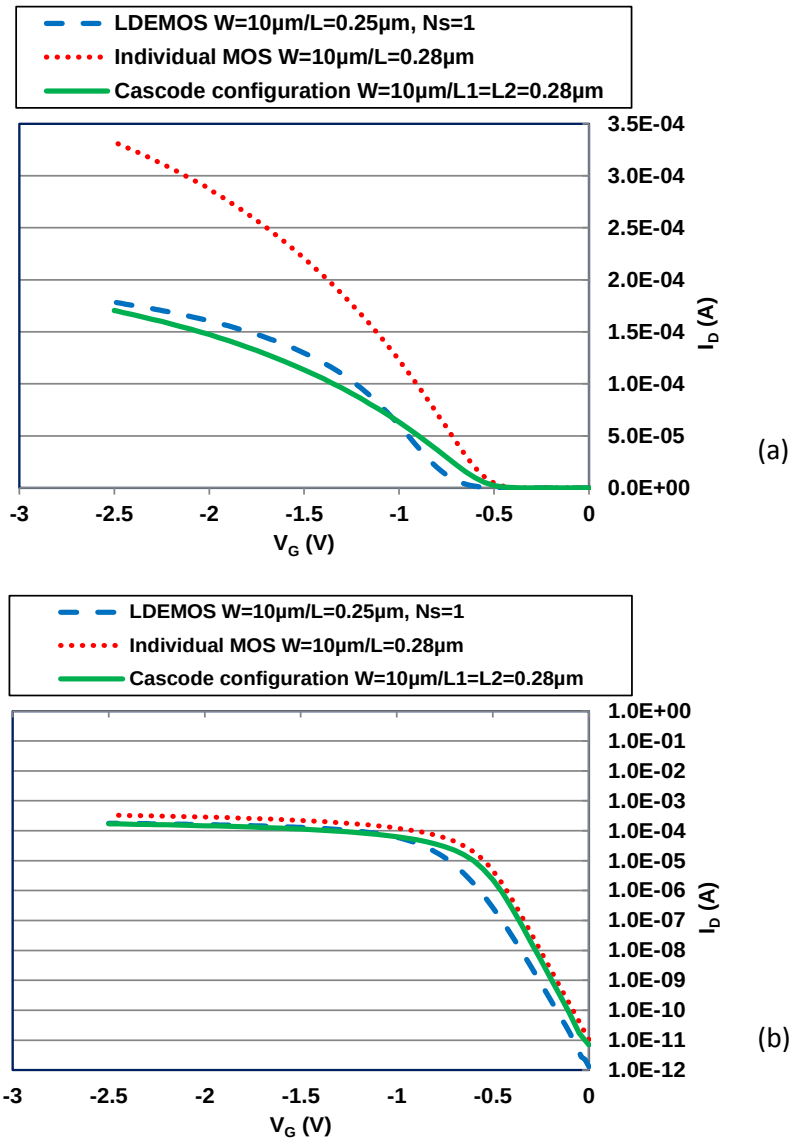


Figure III. 4: Comparison of $I_D(V_G)$ for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in linear regime, plotted with linear scale (a) and Log scale (b).

As the channel length is determined by implantation as opposed to lithography in LDEMOS devices, the LDEMOS |Vt| plot in Figure III. 5 shows a constant characteristic as a function of S. As for individual and cascoded MOS devices, the plots in Figure III. 5 show that the two transistors types have similar |Vt| values across the entire range of S values.

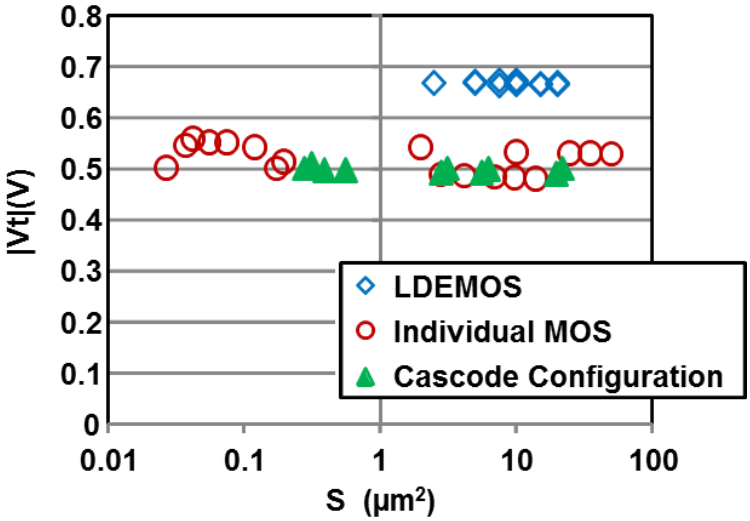


Figure III. 5: Comparison of |Vt(V)| in cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in linear regime.

$iA_{\Delta Vt}$ is then calculated and plotted as a function of S as shown in Figure III. 6. LDEMOS devices show very high $iA_{\Delta Vt}$ values, ranging from 14.9mV.µm for S=15µm^2 to 17.9mV.µm for S=20 µm^2. In the case of individual MOS devices, instead, $iA_{\Delta Vt}$ ranges from 4.1mV.µm for S=25µm^2 to 7.3mV.µm for S=0.126µm^2. It's clear that LDEMOS devices present a high degraded Vt mismatch performance as compared to individual and cascode devices, due to its diffused channel and not well controlled gate length. As plotted in Figure III. 6, cascoded MOSFETs present $iA_{\Delta Vt}$ values ranging from 4.3mV.µm for S=0.28µm^2 to 5.89mV.µm for S=19.6µm^2. This shows that individual and cascoded MOS devices exhibit similar variability performance, both benefiting from an improved robustness to Vt mismatch compared to LDEMOS devices.

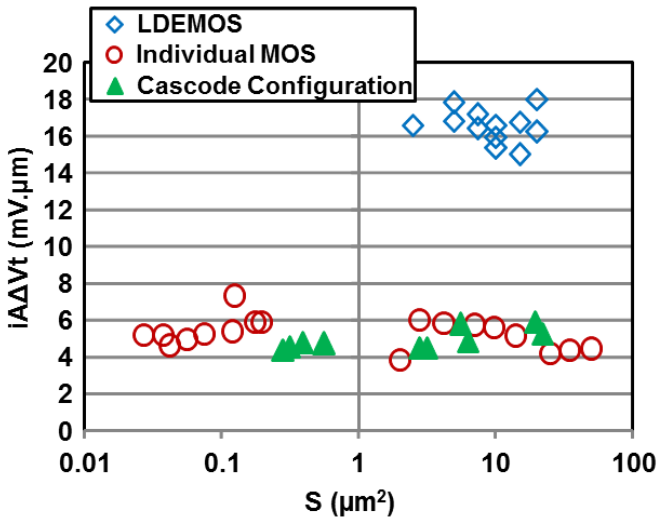


Figure III. 6: Comparison of iAΔVt (mV.µm) for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in linear regime.

The same study was conducted for the current gain factor β. The individual mismatch constants are plotted for all devices as a function of S. The graph reported in

Figure III. 7 shows that, even in this case, MOS devices perform better than LDEMOS, with individual mismatch constants ranging from $iA_{\Delta\beta/\beta}$=2.14%.µm for S=5µm^2 to $iA_{\Delta\beta/\beta}$=3.1%.µm for S=15µm^2 in individual MOS devices and from $iA_{\Delta\beta/\beta}$=1.04%.µm for S=0.175µm^2 to $iA_{\Delta\beta/\beta}$=2%.µm for S=14µm^2 in LDEMOS devices. Again, cascoded and individual MOS devices exhibit similar behaviour, showing improved β mismatch performance compared to LDEMOS devices. Cascoded MOS devices exhibit in fact $iA_{\Delta\beta/\beta}$ values ranging from 0.8%.µm for S=0.392µm^2 to 1.19%.µm for S=19.6µm^2.

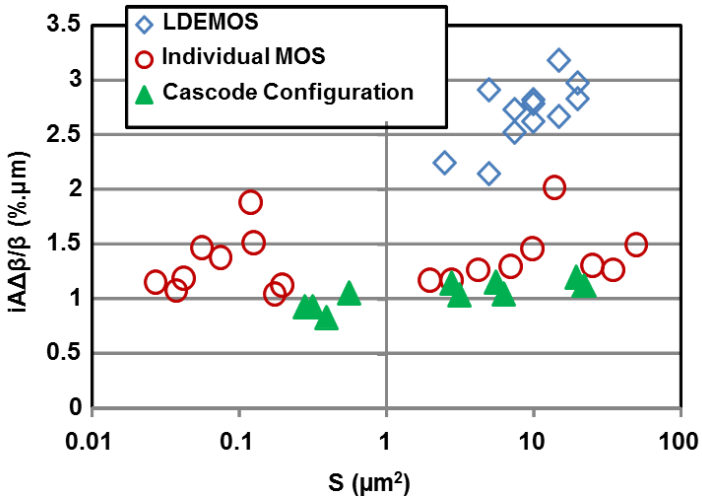


Figure III. 7: Comparison of iAΔβ/β (%.µm) for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in linear regime.

III.3.1.b I_D mismatch

The drain current mismatch was also investigated for the same MOS transistors types and configurations. Figure III. 8 shows that the mismatch in MOS and LDEMOS devices relative to the drain current is not affected by drastic variations, contrary to the mismatch for Vt and β. To understand this phenomenon, Croon's model [Croon 02a] and the improved Croon model proposed in [Rahhal 13] and detailed in chapter II were considered and compared.

As shown in Equation III.1, Croon's model expresses the I_D mismatch as a function of the Vt and β mismatch, their inter-correlation and the term Gm/I_D. This first order model and the improved Croon Model in Equation III.2 were used to describe the observed behaviour of LDEMOS as well as individual and cascoded MOSFET devices. The results are reported in Figure III. 9, Figure III. 10 and Figure III. 11:

- Figure III. 9 shows that for individual MOS devices, Croon's model of Equation III.1 does not reproduce the data relative to small surfaces. The improved Croon model of Equation III.2, instead, reproduces the measured data across the whole range of S. This means that for small surfaces the Rsd term is an important contribution to the drain current mismatch. For big surfaces, instead, this contribution becomes less relevant.
- Figure III. 10 shows that for LDEMOS devices, Croon's model of Equation III.1 does not reproduce the data across the whole range of surface values. A huge gap between the measured data and Equation III.1 is in fact observed. The improved Croon model of Equation III.2, instead, reproduces the measured data across the whole range of S. This means that the Rsd term is an important contribution to the drain current mismatch across the whole range of surface values.
- Figure III. 11 shows that for the cascode configuration, the improved Croon model in Equation III.2 fits the measured data better than Croon's model. However, the gap between Croon's model of Equation III.1 and the measured data is not very pronounced across the whole range of S. Thus the Rsd effect on the drain current mismatch is less pronounced in cascode configuration than in individual and LDEMOS devices.

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{Gm}{I_D}\right)^2.\sigma^2_{\Delta Vt} + \sigma^2_{\Delta\beta/\beta} - 2\frac{Gm}{I_D}\sigma_{\Delta V_T}.\sigma_{\Delta\beta/\beta}.\rho(\Delta Vt, \Delta\beta/\beta) \qquad \textit{(III. 1)}$$

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{Gm}{I_D}\right)^2.\sigma^2_{\Delta Vt} + (1 - Gd.Rsd)^2.\sigma^2_{\Delta\beta/\beta} \qquad \textit{(III. 2)}$$

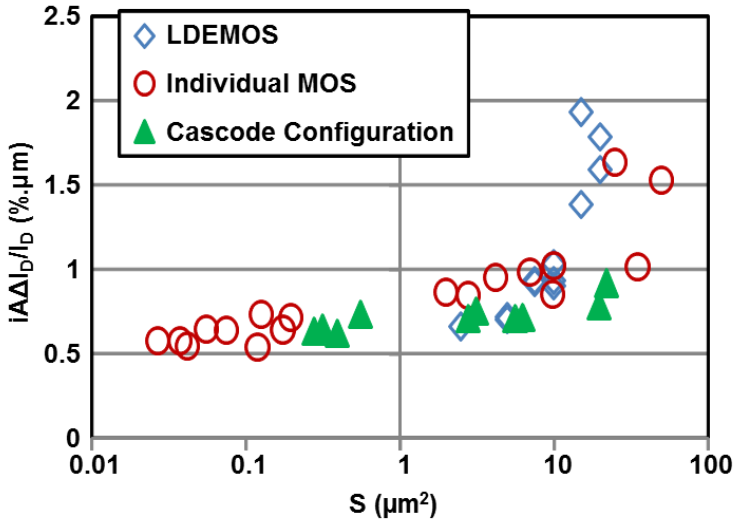


Figure III. 8: Comparison of $iA\Delta I_D/I_D$ (%.µm) for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in linear regime.

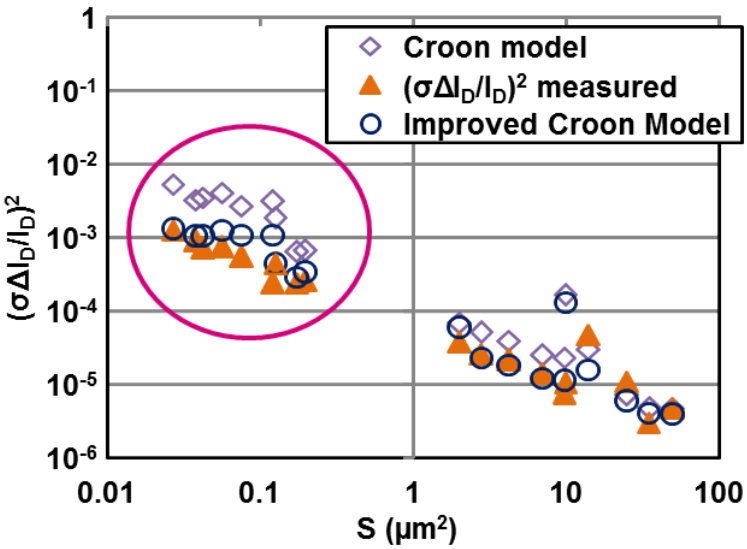


Figure III. 9: Croon's model and improved Croon model applied to the measured data for individual PMOS transistors in linear regime.

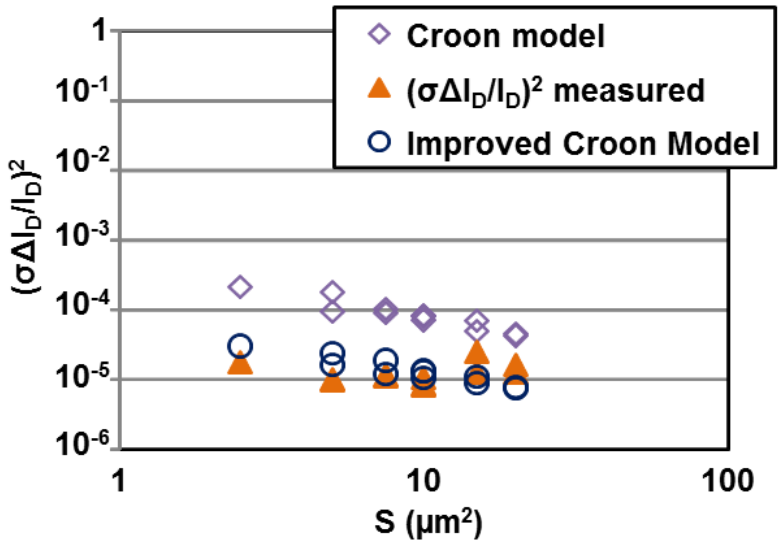


Figure III. 10: Croon's model and improved Croon model applied to the measured data for PLDEMOS transistors in linear regime.

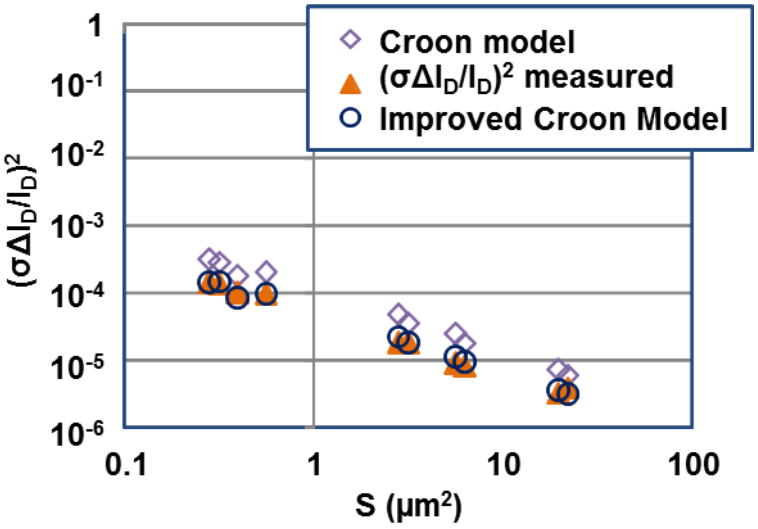


Figure III. 11: Croon's model and improved Croon model applied to the measured data for cascoded PMOS configuration in linear regime.

To fully explain the similarity observed in the I_D mismatch values of LDEMOS, individual and cascoded MOSFETs, the Gm/I_D term was additionally investigated. Figure III. 12 is a plot of Gm/I_D as a function of S for the three devices tested in this study. Individual and cascoded MOS devices perform better in terms of Vt and β mismatch, while at the same time exhibiting almost double Gm/I_D values as compared to LDEMOS devices. Thus the combination of Rsd and Gm/I_D values explains the I_D mismatch similarity between LDEMOS, individual and cascoded MOS devices.

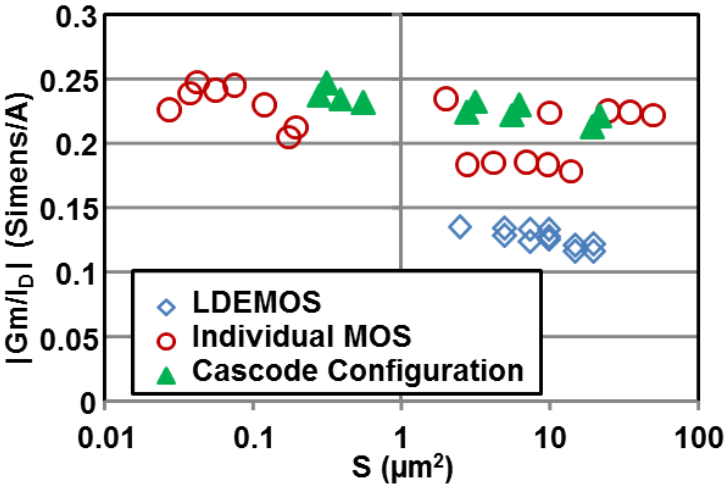


Figure III. 12: Comparison of |Gm/I_D| (Siemens/A) for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in linear regime.

III.3.2 Saturation Regime

Vt, β and I_D were measured in saturation regime at V_G=V_D = -2.5V for individual MOS devices and V_G = -2.5V and V_D=-5V for LDEMOS and cascode configuration devices.
As a first order approximation, the total gate length in the cascode configuration was assumed to be the sum of the gate lengths of the two connected devices.

III.3.2.a Vt mismatch

The $I_D(V_G)$ characteristics were first measured for all devices of the same width W=10µm and specific lengths L (L=0.25µm for LDEMOS device, L=0.28µm for individual MOS devices and L1=L2=0.28µm for cascode configuration devices). The curves reported in Figure III. 13.a show that at maximum |V_G|, LDEMOS devices exhibits higher I_D as compared to individual MOS devices and cascode configuration devices, which exhibits lowest I_D. This result is due to the double gate length of cascode devices as compared to individual and LDEMOS devices. Moreover, the three devices conduct almost the same I_{Doff} current as shown in Figure III. 13.b.

The threshold voltage was measured for all devices using the constant current method proposed by Deen *et al*. [Deen 90] and the absolute values were plotted as a function of the channel area S (µm^2) of the MOS transistors. The obtained results are reported in Figure III. 14. Note that all LDEMOS devices have same gate length (L=0.4µm), same channel length (0.25µm) and different gate widths and number of fingers. The channel length value has been

extracted based on capacitance measurements using the method proposed by Valtonen *et al*. [Valtonen 01].

In saturation regime, the three tested devices exhibit constant and similar |Vt| values as a function of S, as opposed to the linear regime, where LDEMOS exhibits higher |Vt| values compared to individual and cascode configuration devices. This result mainly indicates that LDEMOS devices are affected by high DIBL effects that reduce |Vt| in saturation regime and increase the drain current at high V_G values. Such DIBL effect is clearly observed in Figure III. 15, that shows a comparison of Vt for LDEMOS devices in linear and saturation regime.

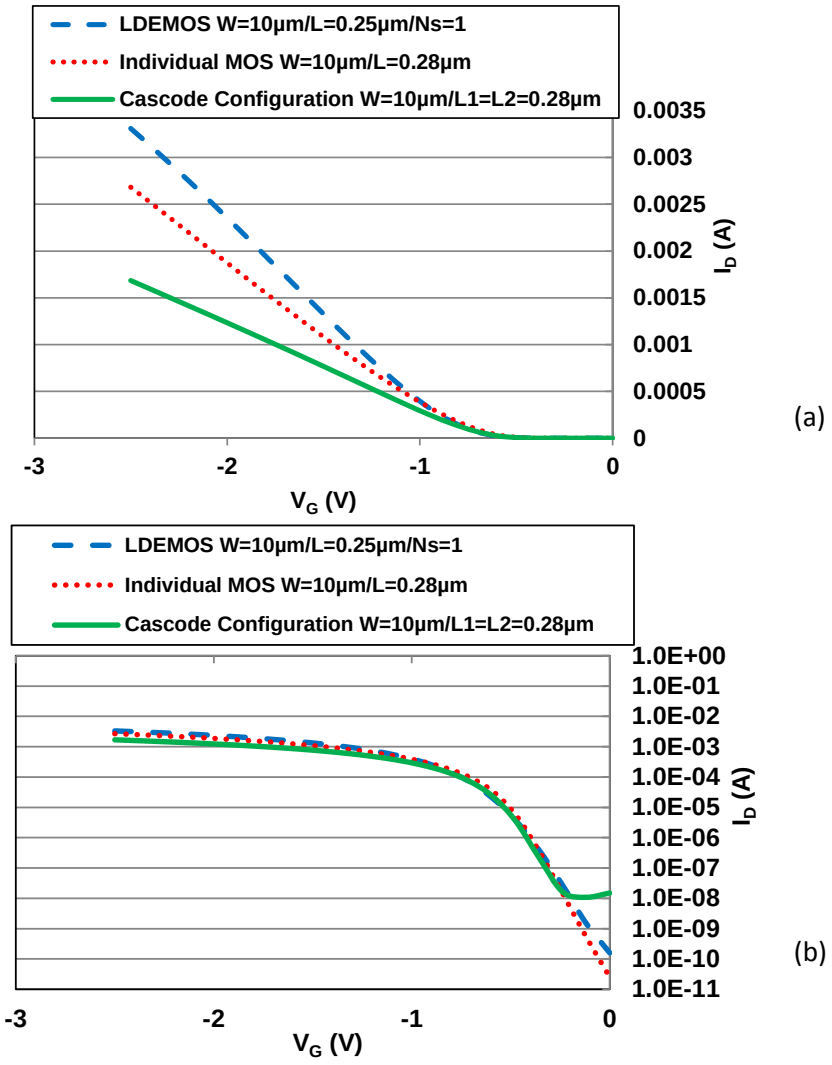


Figure III. 13: Comparison of $I_D(V_G)$ for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in saturation regime plotted in linear scale (a) e in Log scale (b).

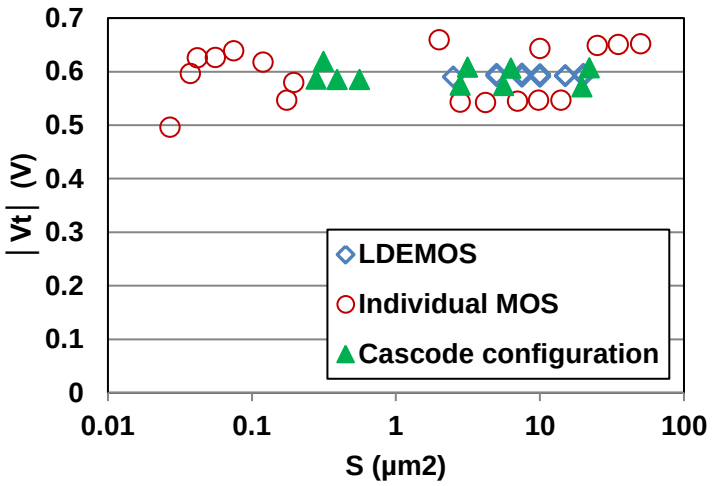


Figure III. 14: Comparison of |Vt(V)| for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in saturation regime.

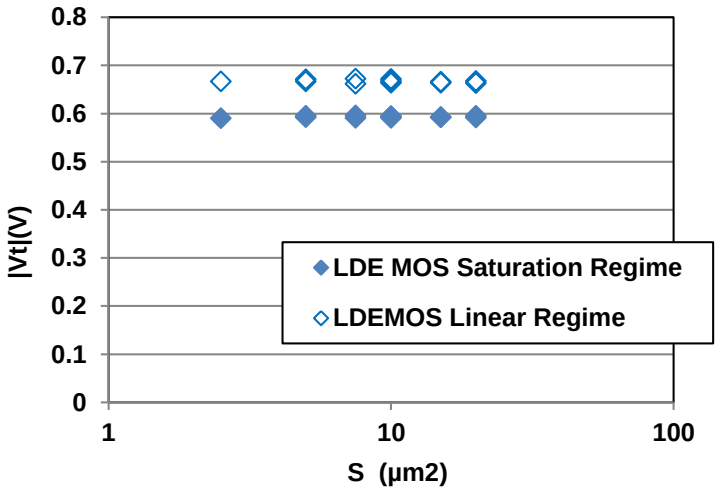


Figure III. 15: Comparison of |Vt(V)| for PLDE MOS devices in linear and saturation regimes.

$iA_{\Delta Vt}$ is then calculated and plotted as a function of S, as shown in Figure III. 16. LDEMOS devices show very high $iA_{\Delta Vt}$ values, ranging from 16.7mV.µm for S=10µm^2 to 17.9mV.µm for S=7.5 µm^2. In the case of individual MOS devices, instead, $iA_{\Delta Vt}$ ranges from 3.4mV.µm for S=25µm^2 to 6.4mV.µm for S=0.027µm^2. By comparing these values, it is clear that the Vt mismatch has a stronger detrimental effect in LDEMOS devices compared to MOS devices also in saturation regime. These results also show that for LDEMOS devices, Vt mismatch is more degraded in saturation regime (iAΔVt around 19 mV.µm) as compared to linear regime (iAΔVt around 16.4 mV.µm). This degradation may be due to DIBL effect.

As plotted in Figure III. 16, cascoded MOSFETs present $iA_{\Delta Vt}$ values ranging from 4.8mV.µm for S=0.315µm^2 to 6.4mV.µm for S=19.6µm^2. This shows that individual and cascoded MOS devices exhibit similar variability performance, both benefiting from an improved robustness to Vt mismatch compared to LDEMOS devices, as well as a less significant DIBL effect.

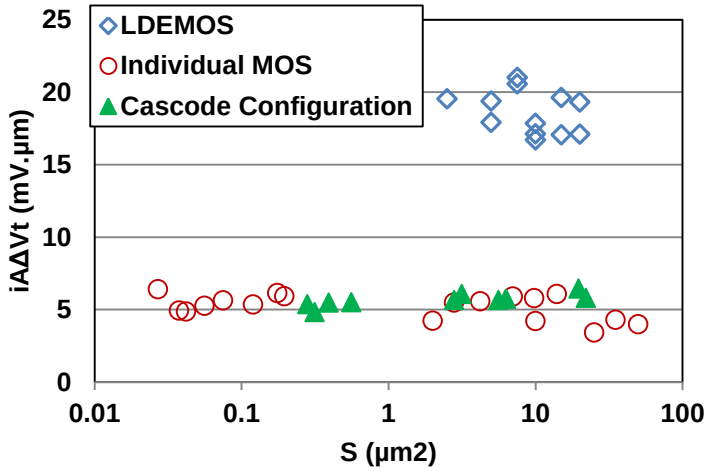


Figure III. 16: Comparison of iAΔVt (mV.µm) for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in saturation regime.

III.3.2.b I_D mismatch

The drain current mismatch was also investigated for the same MOS transistors types and configurations in saturation regime. Figure III. 17 shows that the drain current mismatch in the three devices considered in this study is not affected by drastic variations as opposed to the Vt mismatch. This result is similar to that obtained in linear regime (paragraph III.3.1.b), where the three devices show similar I_D mismatch performances across the whole range of S.

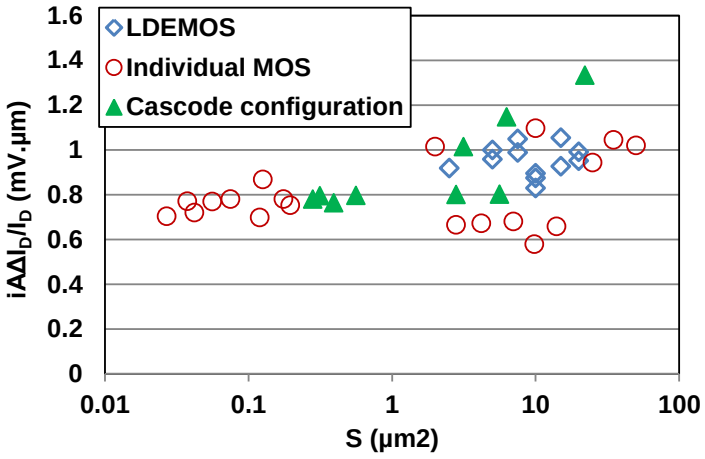


Figure III. 17: Comparison of $iA\Delta I_D/I_D$ (%.µm) for cascoded MOSFETs, individual MOSFETs and PLDE MOS devices in saturation regime.

To try to understand this phenomenon, the same drain current mismatch model approach as chapter II is considered, this time in saturation regime. The drain current equation without the contribution of the source resistance (Rs) can be written as shown in Equation III.3.

$$I_{D0} = \frac{\beta}{2}(V_G - Vt)^2 \qquad \textbf{(III. 3)}$$

The Rs contribution can be assumed as a first order approximation to be Rsd/2. Hence the drain current can be written as shown in Equation III.4.

$$I_D = \frac{\beta}{2}(V_G - Vt - RsI_D)^2 \qquad \textbf{(III. 4)}$$

As for mismatch, by applying the first order Taylor approximation with the hypothesis that the principal contributions to the drain current mismatch in saturation regime are the threshold voltage and the current gain factor, the drain current mismatch can be written as shown in Equation III.5

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{Gm}{I_D}\right)^2 \sigma^2_{\Delta Vt} + \frac{1}{(1+2\beta(V_G - Vt)Rs)} \sigma^2_{\Delta\beta/\beta} \qquad \textbf{(III. 5)}$$

By replacing Rs with Rsd/2, Equation III.5 can be written as shown in Equation III.6, that represents a drain current mismatch model in saturation regime.

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{Gm}{I_D}\right)^2 \sigma^2_{\Delta Vt} + \frac{1}{(1+\beta(V_G - Vt)Rsd)} \sigma^2_{\Delta\beta/\beta} \qquad \textbf{(III. 6)}$$

Croon's mismatch model in Equation III.1 and the new drain current mismatch model in Equation III.6 were applied to the measured data for the three devices considered in this study, and plotted in Figure III. 18, Figure III. 19 and Figure III. 20.

In the case of individual MOS devices, Figure III. 18 shows a small gap between Croon's model and the improved Croon model, compared to the measured data. This gap can be due to the uncertainties in the Rsd extraction technique or to more contributing factors that should be added to the model. This figure also shows that the $\frac{1}{(1+\beta(V_G - Vt)Rsd)} \sigma^2_{\Delta\beta/\beta}$ term is the main contribution to the I_D mismatch.

For the cascode configuration, the same results as individual devices were obtained in Figure III. 20 with no gap between Croon's model and the improved Croon model, compared to the measured data.

The two previous results show that in the case of individual and cascode configuration, the Rsd contribution to the drain current mismatch in saturation is negligible.

Concerning LDEMOS transistors, Figure III. 19 shows that Croon's model and the improved Croon model in saturation regime do not reproduce the data, while the $\left(\frac{Gm}{I_D}\right)^2 \sigma^2_{\Delta Vt}$ term reproduces the measured data across the whole range of S. This proves that this term represents the principal contribution to the I_D mismatch of LDEMOS devices in saturation regime.

All the previous conclusions imply that in saturation regime, while the Vt mismatch is very degraded for LDEMOS as compared to individual devices and devices in cascode configuration, the I_D mismatch for LDEMOS devices joins individual and cascode configuration due to Gm/I_D term.

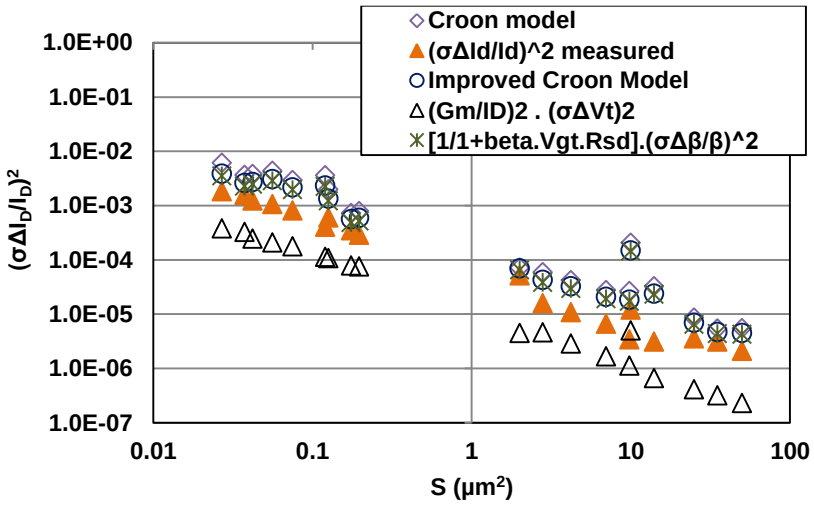


Figure III. 18: Croon's model and improved Croon model applied to the measured data for individual PMOS transistors in Saturation Regime.

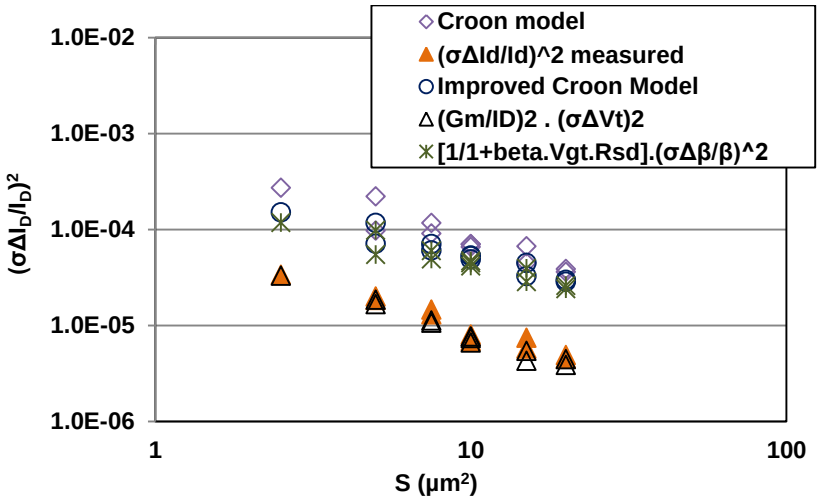


Figure III. 19: Croon's model and improved Croon model applied to the measured data for PLDEMOS transistors in Saturation Regime.

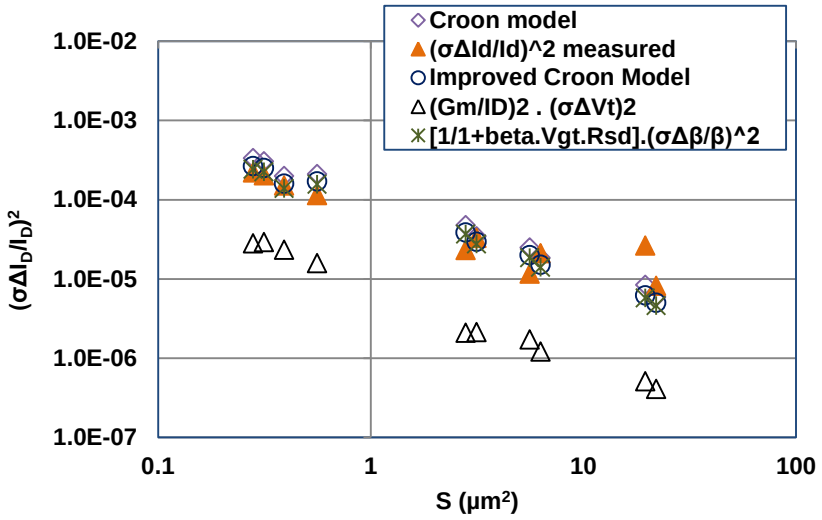


Figure III. 20: Croon's model and improved Croon model applied to the measured data for cascoded PMOS configuration in Saturation Regime.

III.4 Conclusions and perspectives

In the context of designing High Voltage MOSFET devices, by taking into account mismatch issues on top of the classical Ron.Surface/Breakdown trade-off, this work confirms that the LDEMOS architecture is not the optimal candidate architecture. The cascode connection of two MOSFET devices offers improved Vt and β mismatch performances in linear regime, exhibiting characteristics that are very similar to what obtained with individual MOSFETs. The I_D mismatch performances of the cascode configuration are moreover comparable to the characteristics of LDEMOS and individual MOS devices. As for the saturation regime, the Vt values were also shown to be degraded in LDEMOS devices as compared to individual devices and devices in cascode configuration. Degraded results were also obtained in LDEMOS devices in comparison to the linear regime, with highlighted DIBL effect.

As for the drain current, it was shown that the three devices considered in this study exhibit mutually similar and very comparable mismatch performances in saturation regime. A drain current mismatch model was developed for the saturation regime, based on the drain current equation in saturation regime with an Rsd contribution term. This model was applied to the three devices considered in this study. For individual and cascode devices, this model reproduces the experimental data with a certain level of Rsd uncertainty in the case of

individual MOS devices. As for LDEMOS devices, a big gap was observed between the model and the measured data. However, the $(\frac{Gm}{I_D})^2 \sigma^2_{\Delta Vt}$ term in the model was shown to reproduce individually measured data.

For future work, a closer investigation of the three devices can be considered for specific applications. The following two strategies can be devised.

1- The first one is to consider and study LDEMOS, individual MOS devices and devices in cascode configuration having the same drain current values.

   In this case, a comparison of Vt, β and I_D mismatch for the three devices can be considered in linear and saturation regime. Moreover, the area of each device on silicon can be calculated to propose the optimal device for specific applications.

2- The second one is to consider the three devices with the same geometries on silicon. In this case, the drain current values for of each device on silicon can be measured. Moreover, Vt, β and I_D mismatch can also be studied and compared in linear and saturation regimes to propose the optimal device for specific applications.

Chapter IV

Impact of Ge proportions in P-MOSFET channel on matching performances in 28nm Gate first Bulk technology

While chapter II is dedicated to methodology and chapter III to design considerations, this chapter is the first of a series of three dedicated to mismatch contributions and effects in advanced technologies.

In this chapter an exhaustive study of the impact on the mismatch of Vt, β, and I_D of Ge introduction in the channel of bulk 28nm P-MOS transistors is presented. This study is led in parallel on two types of PMOS transistors, i.e. with and without pockets. The interaction between Ge and pocket dopants and its impact on the mismatch properties is also studied.

This chapter is organized in the following sections.

- Section I presents a general introduction of the introduction of Germanium in the MOSFET channel. A state of the art of the influence of Germanium on MOSFET electrical mismatch performances is detailed.
- Section II is dedicated to a description of the experimental setup.
- Section III is focused on MOS transistors without pockets. In this part the matching performances of threshold voltage (Vt), current gain factor (β) and drain current (I_D) measured on devices with and without SiGe are presented.
- Section IV presents the impact of SiGe channel on the Vt, β and I_D matching properties for devices with pocket implants.
- Section V closes the chapter drawing conclusions and devising perspectives.

IV.1 Introduction (State of the art)

Different techniques have been introduced to boost the transistors performances such as the introduction of Germanium (Ge) in the P-MOS channel. The fully strained SiGe channel grown on Si substrates has been demonstrated to tune the threshold voltage (Vt) [Takagi 08] [Krishnamohan 06] [Harris 07] [Lee 09] [Khakifirooz 11] and to boost the hole mobility [Goto 93] [Verdonckt 94] [Voinigescu 94] of P-MOS transistors.

Different studies have been conducted on the influence of SiGe on the electrical transport parameters in P-MOS transistors [Yeo 05] [Clavelier 07] [De Jaeger 07] [Hellings 10]. However, increasing the Ion of the devices is not the only challenge. Many blocks such as SRAM or Analog-Digital converters are based on the availability of electrically matched pairs of transistors [Hu 04] [Boeuf 08] [Bhavnagarwala 05] [Saxena 08]. Studying the impact of SiGe channel on the matching properties of PMOS transistors is therefore mandatory.

Some studies have been led on the variations of electrical parameters affected by the presence of Germanium in P-MOS channel. Yuan in [Yuan 12] showed that the presence of Ge in the P-MOS channel introduces an additional variability source and degrades the Vt mismatch, while Le Royer in [Le Royer 11] showed that in SOI P-MOSFET's, the introduction of Ge in the channel does not degrade the Vt variability.

In this work, P-MOS transistors of 28nm Bulk technology integrating High K/Metal gate and SiGe channel are considered. An exhaustive study of the Vt, β, and I_D mismatch with different Ge proportions in the channel is performed in linear regime for transistors with and without pocket implants. A comparison between channels with and without Germanium and with different proportions of Germanium is also presented.

IV.2 Experimental setup

Electrical characterizations have been carried out on 28nm Bulk transistors with and without pocket implant, where a SiGe channel of 7nm thickness is grown on Si substrates as shown in Figure IV. 1. These transistors integrate High-k gate oxide and TiN metal gate with 0.03µm nominal designed channel length and oxide thickness of 1.71nm.

Tests have been performed in linear regime with drain voltage $|V_D|$ = 0.05V and gate voltage $|V_G|$ in the range of 0 - 1V. All presented results refer to measurements performed at 25°C.

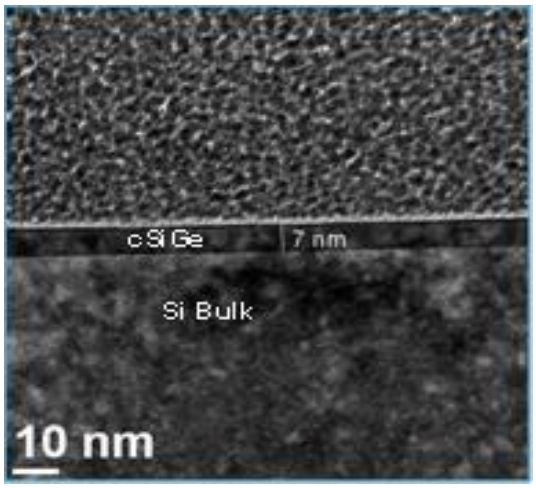


Figure IV. 1: SiGe channel (thickness=7nm) grown on Si Substrate (thickness=10nm)

For matching measurements, a sample of 75 pairs of identical MOS transistors has been considered, laid in the mismatch test structures of Section I.5.2. Note that all transistors belong to the same lot, with one wafer per Ge content, including no germanium (W/O Ge).

For matching studies, the statistical processing described in section I.4 is applied:

- An electrical parameter P is measured for each of the two paired devices.
- The difference of P noted ΔP (or ΔP/P) between the pair is calculated.
- This method is then repeated for the 75 samples present on each wafer.
- A recursive filter is then applied to this population to remove erroneous data. The number of rejects is comprised between 0 and 5 for all tested wafers presented in this work.
- Once the distribution after filtering has been verified to be Gaussian and centered on 0, the standard deviation $\sigma_{\Delta P}$ (or $\sigma_{\Delta P/P}$) of the distribution is calculated.

In this work the individual mismatch constant of Equation I.29 is considered. This parameter allows the evaluation of the mismatch values for each channel dimension (Section I.4.5.c).

IV.3 Electrical parameters mismatch characterization on transistors without pocket implants

IV.3.1 Threshold Voltage mismatch

For transistors with and without Ge, the threshold voltage is extracted using the maximum slope method with $|V_D|$=0.05V [Hao 85]. The $|Vt|$ values are plotted in Figure IV. 2 as a function of the length of the transistors (L). Figure IV. 2 shows that for small lengths (L<0.24µm), a short channel effect (SCE) is observed, while for long lengths (L≥0.24 µm), $|Vt|$ is constant. Figure IV. 2 also shows that $|Vt|$ decreases when the Ge percentage increases.

The reduction of $|Vt|$ with the Ge introduction in the MOSFET channels is explained in [Fischetti 96] and shown in Figure IV. 3. When Ge is introduced, the valence band is shifted upwards while the conduction band is almost invariable, thus reducing the band gap. This reduction implies that the Fermi level and the intrinsic Fermi level are shifted upwards and thus the semiconductor work function (ϕ_{SC}) is reduced. Finally, the ϕ_{SC} reduction induces a $|Vt|$ decrease, as shown in Equations IV.1 & IV.2.

$$Vt = 2\phi_F + V_{FB} + \frac{Q_d}{C_{ox}} \qquad \textbf{(IV. 1)}$$

$$V_{FB} = \phi_m - \phi_{SC} \Rightarrow |Vt_{SiGe}| < |Vt_{Si}| \qquad \textbf{(IV. 2)}$$

Where ϕ_F is the Fermi potential, V_{FB} is the flat band voltage, Q_d is the depletion charge, C_{ox} is the gate oxide capacitance, ϕ_m is the metal work function and ϕ_{SC} is the semiconductor work function. The $|Vt|$ shift as a function of the Ge percentage is well known and explained in [Weber 89].

The individual constants of Vt matching have been calculated and plotted as a function of L in Figure IV. 4. In this figure we observe that the Vt matching performances are not affected by the presence of Ge in the percentage range considered in this study. Indeed, the Ge presence in the channel may induce two additional contributions: the variation of SiGe layer thickness (T_{SiGe}) and the variation of the valence band (Ev) level.

Concerning the first one, it has been shown in [Soussou 12] that the T_{SiGe} (7nm in our case as shown in Fig.1) is large enough (T_{SiGe} > 5nm), thus the induced Vt variations are negligible.

The impact of Ev level variations on the Vt mismatch is more complex. Assuming that the number of Ge atoms in the channel has the same behavior than dopants i.e. governed by a Poisson law, the individual constant of matching due to Ev level variations can be written as in Equation IV.3.

$$iA_{Ev}(Ge) = \frac{\Delta E_V}{\Delta X} \cdot \frac{\sqrt{X}}{\sqrt{T_{SiGe}.N(Ge)}} \qquad \textbf{(IV. 3)}$$

Where $\frac{\Delta E_V}{\Delta X}$ is the slope of band offset E_V as a function of Germanium content X [Soussou 12], i.e. $\frac{\Delta E_V}{\Delta X} = 0.66eV$, X is the Germanium percentage, T_{SiGe} is the SiGe layer thickness and $N(Ge)$ is the germanium concentration $(N(Ge) = 4.4 \times 10^{22} at/cm^3)$

Using Equation IV.3, Table IV.1 shows that for the percentages of Ge considered, $iA_{Ev}(\%Ge)$ is not sufficiently large to create a significant difference to the Vt mismatch. The negligible influence on $iA_{\Delta Vt}$ due to the presence of Ge is also verified in Figure IV. 5, where no remarkable Vt mismatch difference is observed between the maximum and the minimum percentages of Ge.

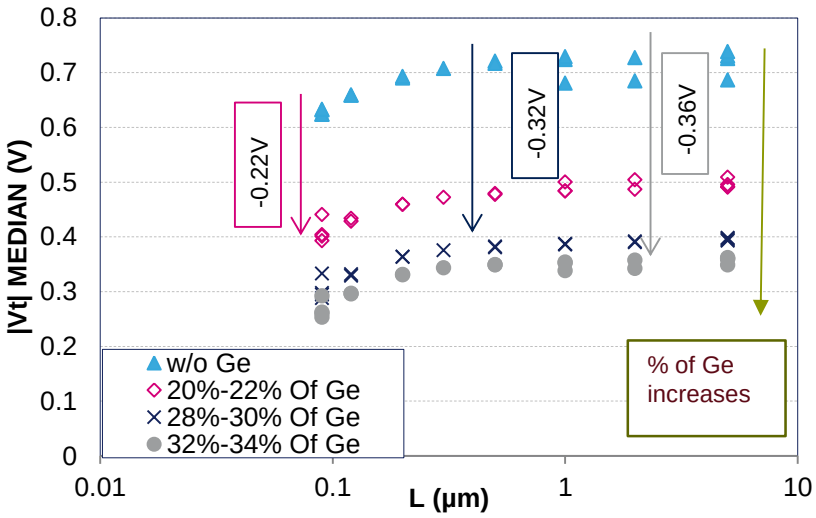


Figure IV. 2: Transistors without Pockets: Threshold voltage values as a function of L, for channels without Ge and for different percentages of Ge

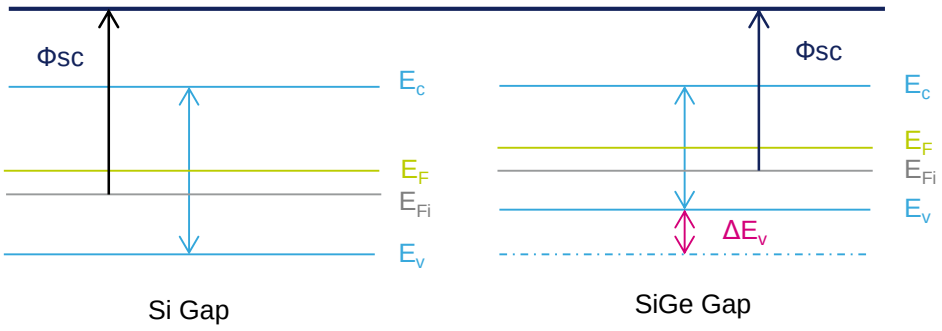


Figure IV. 3: An illustration of the effect of the Ge introduction on the energy bands of the semiconductor

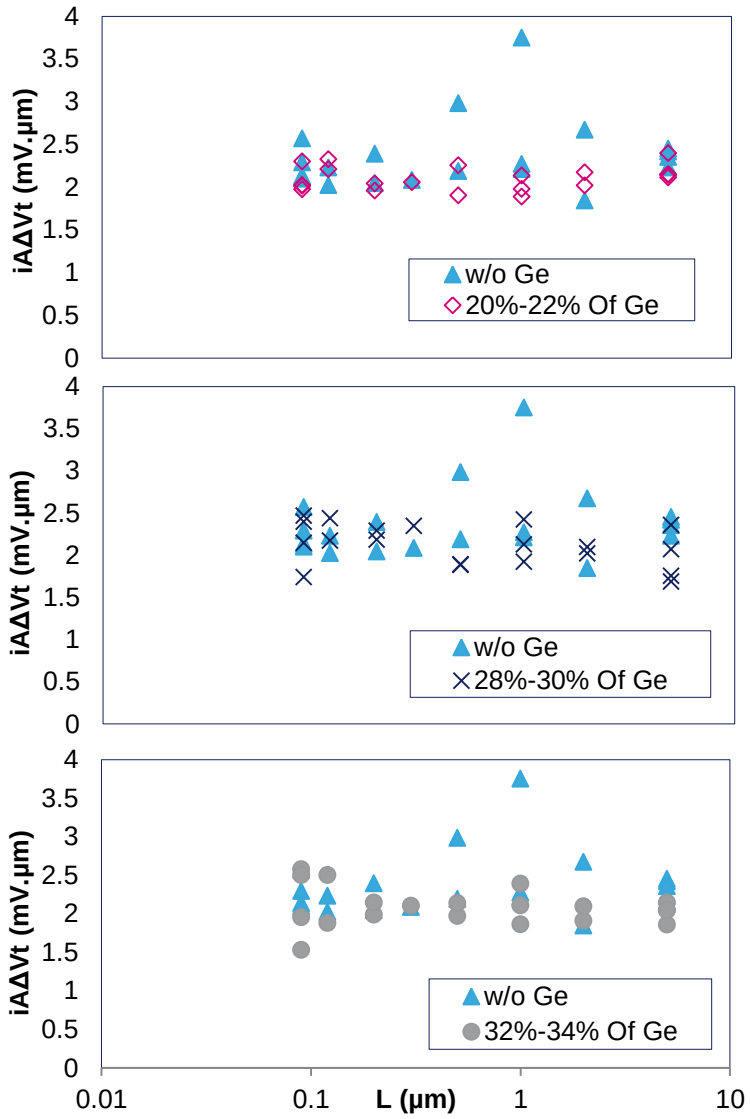


Figure IV. 4: Transistors without Pockets: Comparison of iAΔVt as a function of L between transistors without and with different percentages of Ge

Table IV.1: iA_{Ev} (%Ge) values for different percentages of Ge derived from Equation IV.3.

Percentage of Ge	iA_{Ev} (%Ge) (eV.µm)
20% - 22% of Ge	$1.699x10^{-5}$ eV.µm
28% - 30% of Ge	$2.01x10^{-5}$ eV.µm
32% - 34% of Ge	$2.149x10^{-5}$ eV.µm

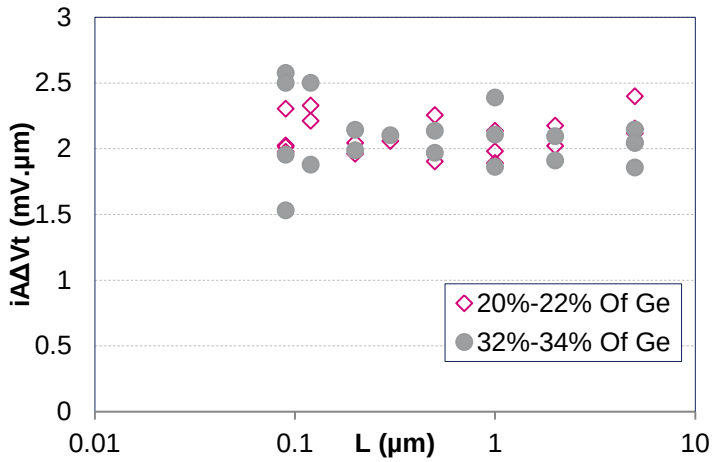


Figure IV. 5: Transistors without Pockets: Comparison of $iA_{\Delta Vt}$ as a function of L between the minimum and the maximum considered percentages of Ge

IV.3.2 Current gain factor mismatch

The current gain factor β is extracted using the maximum slope method with $|V_D|$=0.05V [Hao 85]. The β individual constants of matching are then calculated and plotted as a function of L in Figure IV. 6, for transistors without and with different percentages of Ge. This figure clearly exhibits an improvement in the β mismatch performances when Ge is introduced in the channel. Moreover, no significant variation of $iA_{\Delta\beta/\beta}$ is observed as a function of the Ge percentage between 20% and 34% as shown in Figure IV. 7.

The mobility improvement with Ge introduction is the object of different studies and publications such as [Goto 93] and [Krishnan 11], which attribute this beneficial effect to an improved carrier effective mass. A recent study [Diouf 13] that uses the same samples characterized in this work has highlighted that the low field mobility (μ_0) enhancement is higher than expected. The additional mobility improvement was explained by fewer Coulomb

scattering events (charges at the SiGe/SiO_2 interface, defects or traps in the dielectric) when Ge is introduced.

Back to mismatch issues, Difrenza in [DiFrenza 02a] showed that the major sources of β variability related to low field mobility are the local fluctuations in the number of dopants in the channel and the charges trapped at the Si/SiO_2 interface. This suggests that, in our case, when the charges at the SiGe/SiO_2 interface are reduced, the β mismatch could be improved as it is observed.

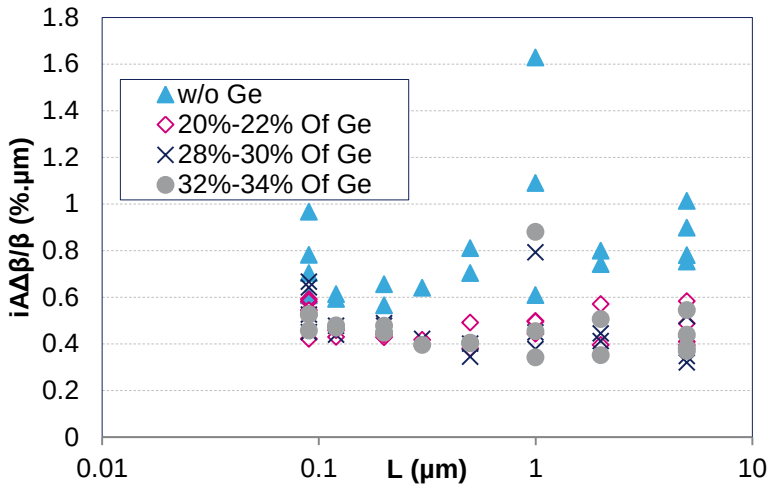


Figure IV. 6: Transistors without Pockets: Comparison of $iA_{\Delta\beta/\beta}$ as a function of L between transistors without and with different percentages of Ge

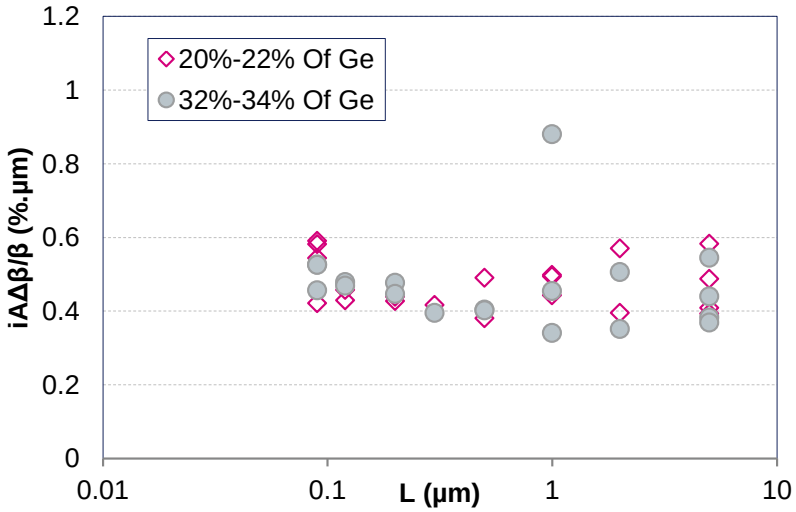


Figure IV. 7: Transistors without Pockets: Comparison of $iA_{\Delta\beta/\beta}$ as a function of L between the minimum and the maximum considered percentages of Ge

Finally, while in [Diouf 13] the authors observed an improvement in μ_0 when the Ge content is increased, Figure IV. 7 does not show any significant variation of $iA_{\Delta\beta/\beta}$ between 20% Ge and 34% Ge. This indicates that, while μ_0 improvement depends on the dielectric charges and the carriers' effective mass (known to be improved when the percentage of Ge is increased), β mismatch depends only on dielectric charges, as expected.

IV.3.3 Drain current mismatch

The drain current (I_D) values are extracted in linear mode at $|V_G|$=1V and $|V_D|$=0.05V. I_D/W values are then plotted as a function of L. Figure IV. 8 shows that I_D/W increases with the introduction of Ge and when its percentage increases. Indeed, this is directly related to the $|Vt|$ reduction, increasing the gate voltage drive, and, also to the μ_0 improvement with the Ge content.

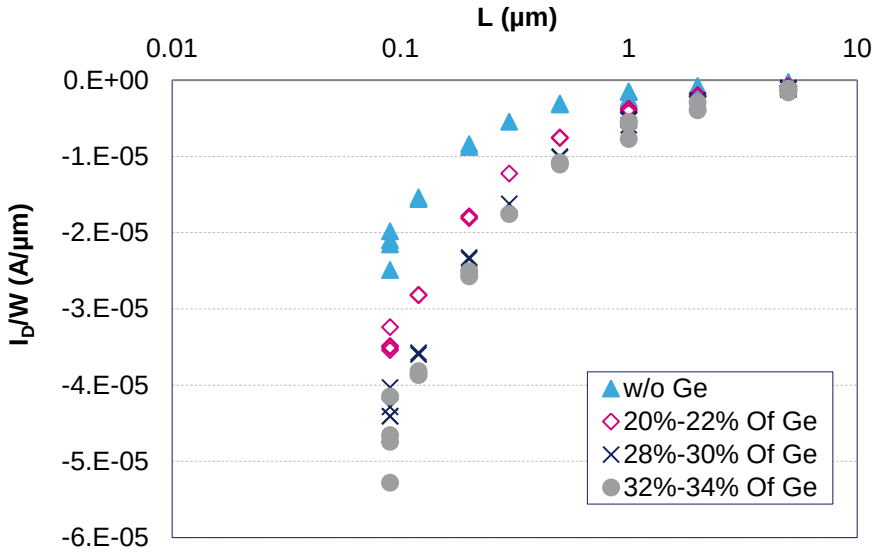


Figure IV. 8: Transistors without Pockets: I_D/W as a function of L, for channels without Ge and with different Ge percentages

$iA_{\Delta ID/ID}$ is plotted as a function of L in Figure IV. 9, showing that when Ge is added in the P-MOS channel, the I_D mismatch is improved. Moreover, the I_D mismatch exhibits higher improvement as the Ge percentage is increased.

In order to explain the current mismatch improvement, Croon's model with correlation [Croon 02a] of Equation IV.4 is considered

$$iA^2_{\Delta I_D/I_D} = (\frac{Gm}{I_D})^2 . iA^2_{\Delta Vt} + iA^2_{\Delta\beta/\beta} - 2.(\frac{Gm}{I_D}) . iA_{\Delta Vt} . iA_{\Delta\beta/\beta} . correl(\Delta Vt, \Delta\beta/\beta) \quad \textbf{(IV. 4)}$$

This model is applied to the measured data for transistors without and with Germanium.

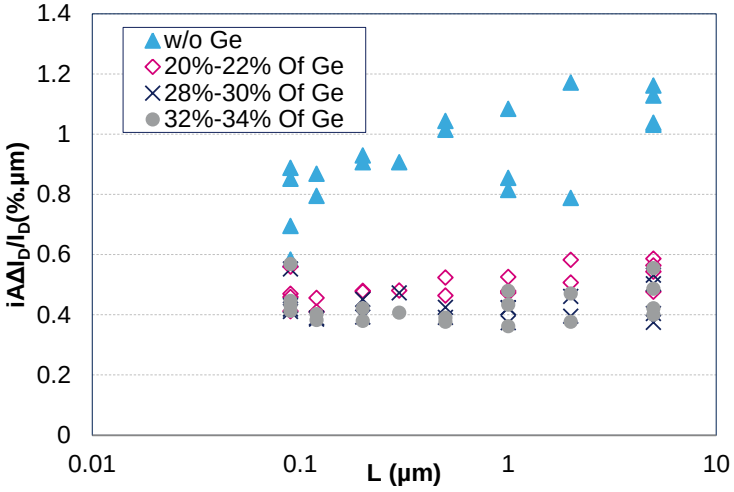


Figure IV. 9: Transistors without Pockets: Comparison of $iA_{\Delta ID/ID}$ as a function of L between transistors without and with different percentages of Ge.

A comparison of $iA^2_{\Delta ID/ID}$ as a function of L between the measured data and Croon's model is shown in Figure IV. 10 for transistors without Ge and in Figure IV. 11 for transistors with 20-22% of Ge. The two cases show that this model provides a good fit, implying that, for both transistors without and with Ge, the drain current mismatch is the result of a combination of Vt and β mismatch effects plus their correlation. Thus, an improvement in one of these parameters induces an improvement in the current mismatch. In this case, the β mismatch improvement explains the lower drain current variability observed in transistors with Germanium. Moreover, Equation IV.4 shows that $iA^2_{\Delta ID/ID}$ depends of $(\frac{Gm}{I_D})^2$, thus when the absolute value of I_D is increased, I_D mismatch is improved, explaining the improvement of I_D mismatch in Figure IV. 12 with the Ge percentage increase.

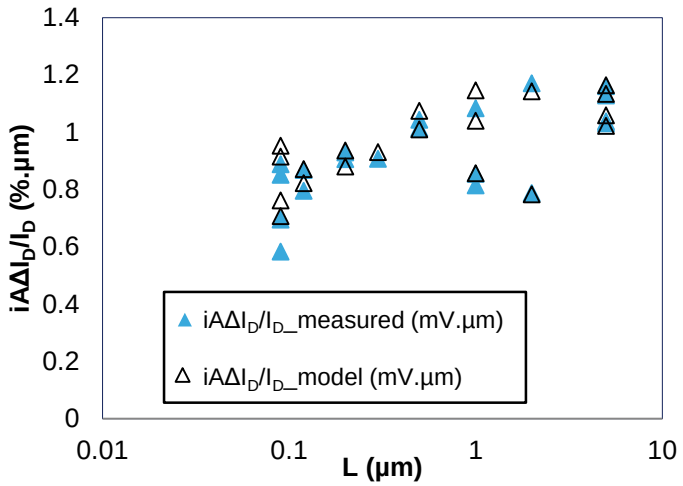


Figure IV. 10: Transistors without Pockets: Current variability from Croon's model compared to the measured current variability for transistors without Ge.

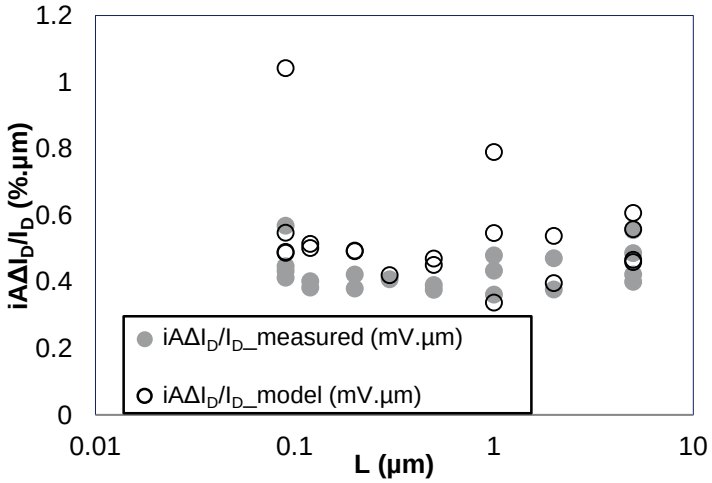


Figure IV. 11: Transistors without Pockets: Current variability from Croon's model compared to the measured current variability for transistors with Ge.

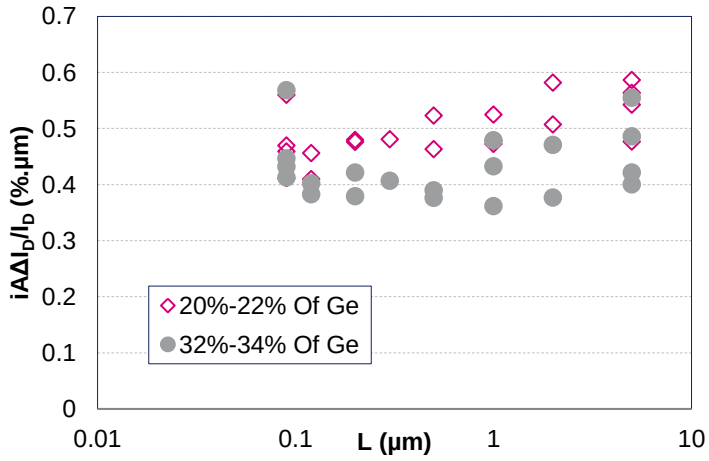


Figure IV. 12 Transistors without Pockets: Comparison of $iA\Delta I_D/I_D$ as a function of L between the minimum and the maximum considered percentages of Ge.

IV.4 Electrical parameters mismatch characterization on transistors with heavily pocket implants

IV.4.1 Threshold Voltage mismatch

In this section we consider devices with pockets (type: Arsenic) implanted in the channel. For transistors with and without Ge, the threshold voltage is extracted using the maximum slope method with |Vd|=0.05V [Hao 85]. The $|Vt|$ values are plotted in Figure IV. 13 as a function of the length of the transistors (L). Contrary to MOS transistors without pockets, no SCE is observed and $|Vt|$ increases when L decreases. Figure IV. 13 also shows that when the percentage of Ge is increased, $|Vt|$ decreases.

The reduction of $|Vt|$ with the introduction of Ge in the MOSFET channels is due to the valence band shift as explained in paragraph IV.3.1.

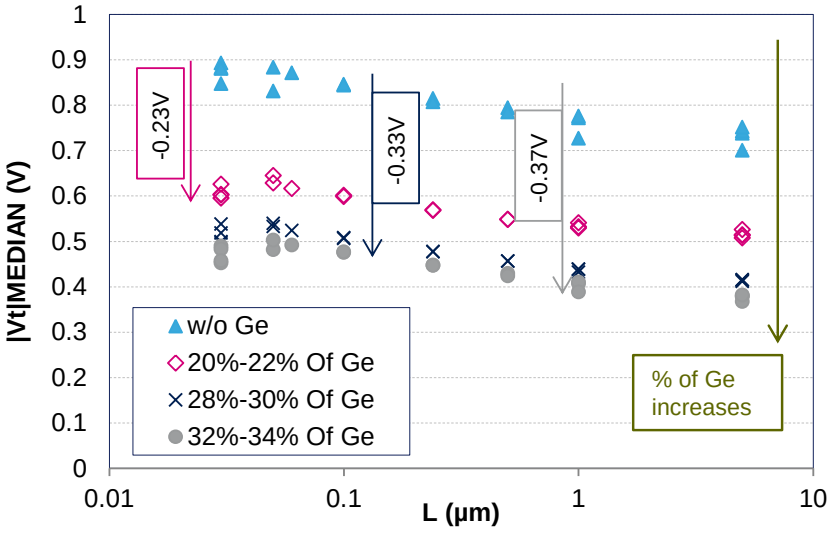


Figure IV. 13: Transistors with Pockets: Threshold voltage values as a function of L, for channels without Ge and for different percentages of Ge.

The individual constants of Vt matching have been calculated and plotted as a function of L in Figure IV. 14. For transistors without Ge, $iA_{\Delta Vt}(L)$ has the typical shape of MOS transistors with pockets [Mezzomo 10c]. When Ge is added, $iA_{\Delta Vt}(L)$ exhibits the same shape as MOS transistors with pockets, with less degradation at $L \geq 1\mu m$.

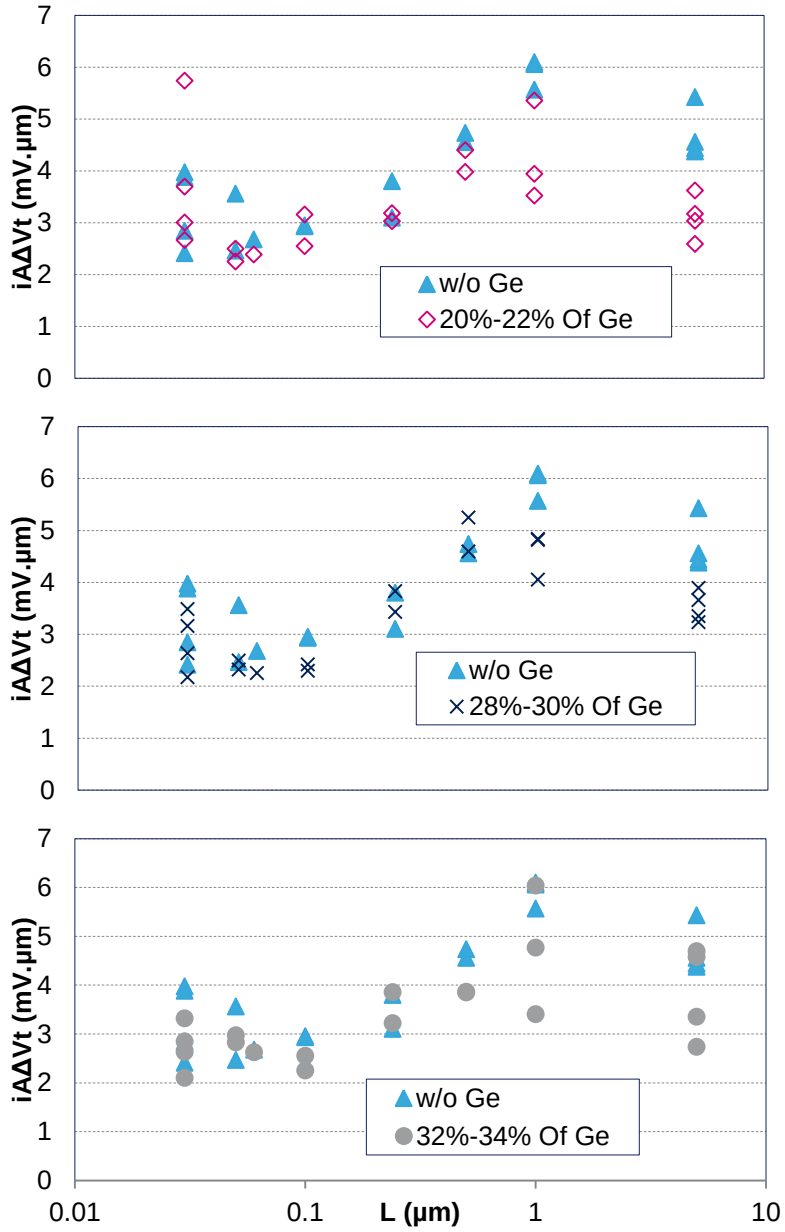


Figure IV. 14: Transistors with Pockets: Comparison of $iA_{\Delta Vt}$ as a function of L between transistors without and with different percentages of Ge.

The authors in [Mezzomo 10c] have demonstrated that for short transistors, a higher level of pocket doping induces mismatch degradation. As for long transistors, in addition to the pocket doping level, if the contrast between the pockets and the rest of the channel is increased, the Vt mismatch is degraded.

The improvement of Vt mismatch for L≥1µm suggests that the presence of Ge promotes the diffusion of Arsenic in the channel [Liu 03]. This diffusion causes larger and more

dispersed pockets. Thus, the contrast between the pockets and the rest of the channel is reduced, as shown in Figure IV. 15, inducing less degradation at L≥1µm.

Figure IV. 16 shows no significant variation of $iA_{\Delta Vt}$ when the percentage of Ge is increased. Thus no impact on the Vt mismatch performance is observed for Ge contents between 20% and 34%, suggesting that the percentage of Ge is not sufficient to generate differences.

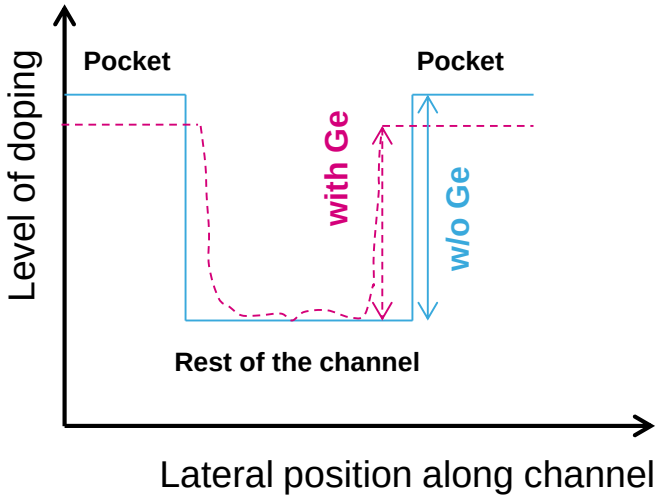


Figure IV. 15: An illustration of the contrast between the pocket doping and the rest of the channel in the case of transistors with and without (W/O) Ge.

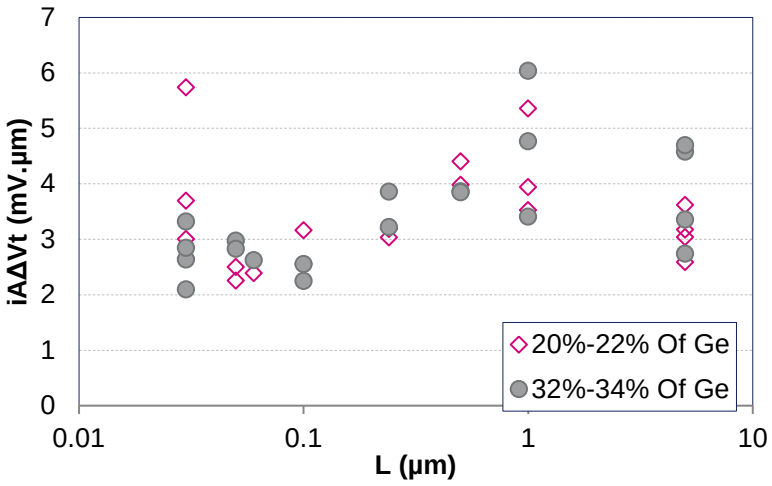


Figure IV. 16: Transistors with Pockets: Comparison of $iA_{\Delta Vt}$ as a function of L between the minimum and the maximum considered percentages of Ge.

It is known that in poly-gate technology, nFET exhibit significantly higher $iA_{\Delta Vt}$ than pFET. To verify if this is also the case for High K/Metal gate technology, tests have been

conducted on NMOS Bulk transistors with pocket doping. The $iA_{\Delta Vt}$ mismatch results show similar values and behavior in NMOS and PMOS devices with pocket doping, with the introduction of Ge as shown in Figure IV. 17:

- Hump at L=1µm: $iA_{\Delta Vt}$ value is equal to 5.1 mV.µm.

This suggests that with the introduction of Germanium and the use of metal Gate technology, the previously observed higher $iA_{\Delta Vt}$ in nFET with respect to pFET is not any more relevant. Instead, nFET and pFET devices exhibit very similar $iA_{\Delta Vt}$ values.

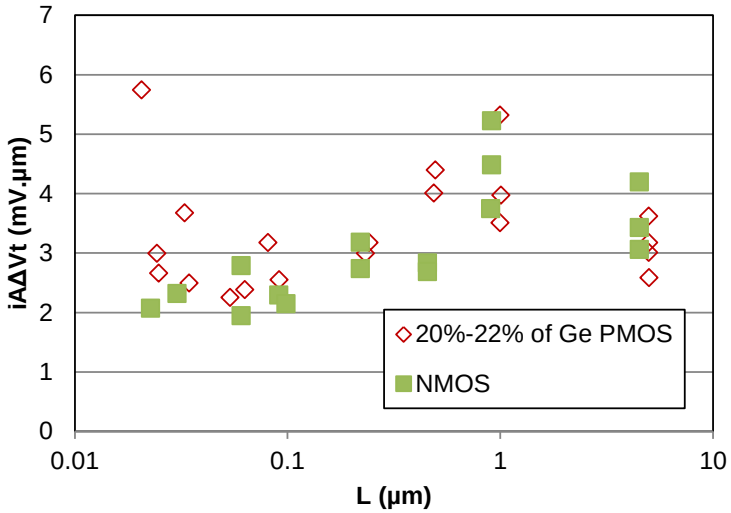


Figure IV. 17: Comparison between NMOS and PMOS (with Ge) Vt mismatch as a function of L.

IV.4.2 Current gain factor mismatch

The current gain factor β is extracted using the maximum slope method with $|V_D|$=0.05V [Hao 85]. The β individual constants of matching are then calculated and plotted as a function of L in Figure IV. 18 for transistors without and with different percentages of Ge. This figure shows an improvement in β mismatch with the introduction of Ge. The same considerations as paragraph IV.3.2 apply, suggesting that when the Coulomb scattering (charges at the $SiGe/SiO_2$ interface, defects or traps in the dielectric) is decreased due to Ge introduction, β mismatch is improved.

Moreover between 20% Ge and 34% Ge, no significant variation of $iA_{\Delta\beta/\beta}$ is observed, as shown in Figure IV. 19. This suggests that, while the μ_0 improvement [Diouf 13] depends

on the dielectric charges and the carriers' effective mass (known to be improved when the percentage of Ge is increased), the β mismatch depends only on dielectric charges.

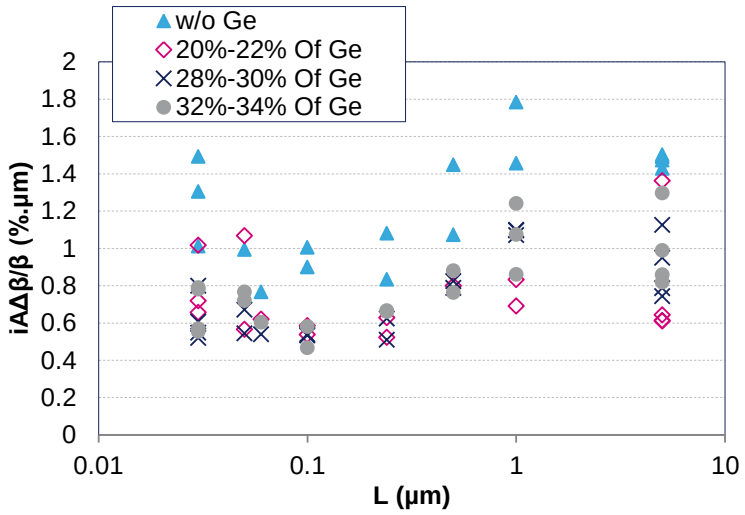


Figure IV. 18: Transistors with Pockets: Comparison of $iA_{\Delta\beta/\beta}$ as a function of L between transistors without and with different percentages of Ge.

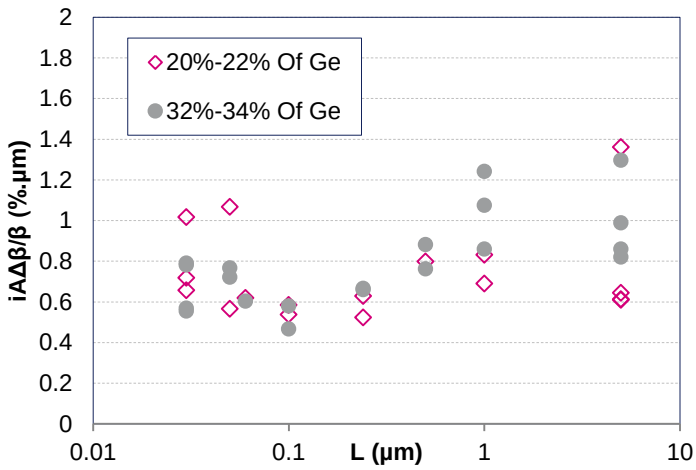


Figure IV. 19: Transistors with Pockets: Comparison of $iA_{\Delta\beta/\beta}$ as a function of L between the minimum and the maximum considered percentages of Ge.

IV.4.3 Drain current mismatch

The drain current (I_D) values are also extracted in linear mode at $|V_G|$=1V and $|V_D|$=0.05V. I_D/W is then plotted as a function of L in Figure IV. 20, showing again that the

I_D/W values increase with the introduction of increasing Ge content, due to the Vt reduction and mobility improvement.

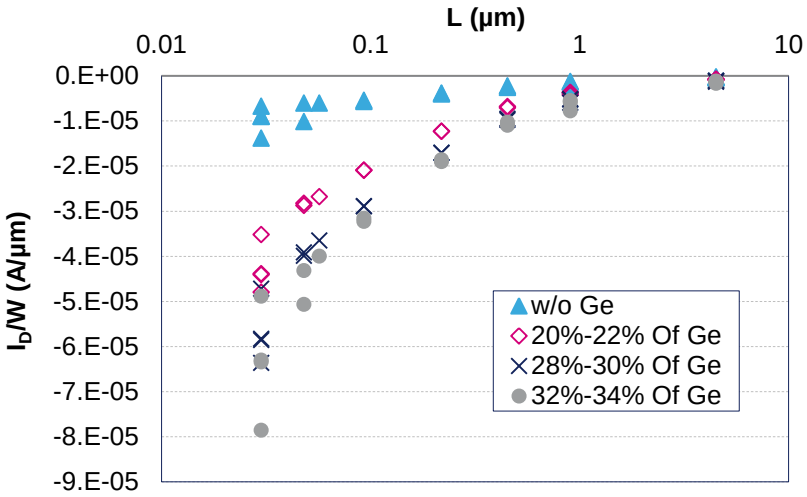


Figure IV. 20: Transistors with Pockets: I_D/W as a function of L, for channels without Ge and for different percentages of Ge

Similarly, $iA_{\Delta I_D / I_D}$ is plotted as a function of L in Figure IV. 21. This figure shows that when Ge is added in the P-MOS channel, the I_D mismatch is improved. Moreover, the I_D mismatch exhibits higher improvement at higher Ge percentages, as shown in Figure IV. 22.

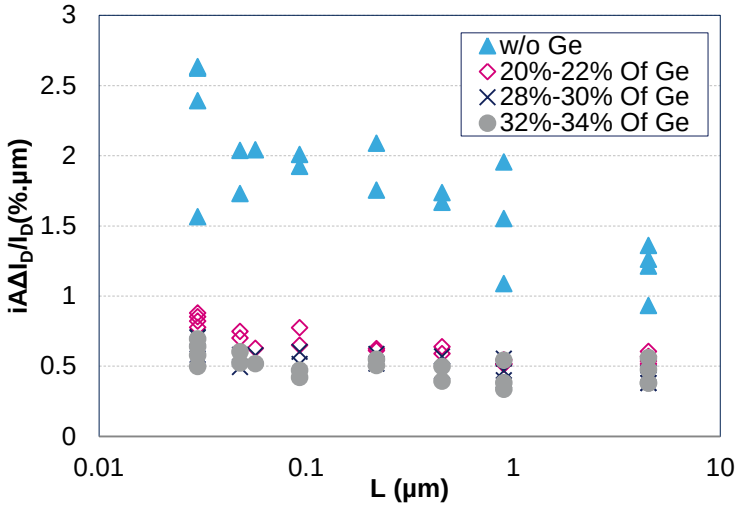


Figure IV. 21: Transistors with Pockets: Comparison of $iA_{\Delta ID/ID}$ as a function of L between transistors without and with different percentages of Ge

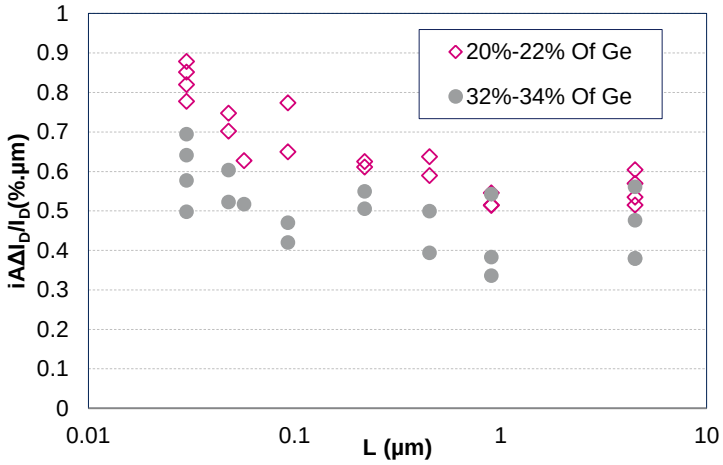


Figure IV. 22: Transistors with Pockets: Comparison of $iA_{\Delta ID/ID}$ as a function of L between the minimum and the maximum considered percentages of Ge

In order to explain the current mismatch improvement, Croon's model expressed by Equation IV.4 is again applied to the measured data for transistors without and with Germanium. A comparison of $iA^2_{\Delta I_D / I_D}$ as a function of L for the measured data and Croon's model is presented in Figure IV. 23 for transistors without Ge and in Figure IV. 24 for transistors with 32-34% Ge. Figure IV. 23 shows that, for channels without Ge, Croon's model offers a good fit. As for transistors with Ge, in Figure IV. 24, Croon's model overestimates the measured values. This underestimation suggests that, for SiGe channels, in addition to Vt, β mismatch and their correlation, more terms should be considered, such as the Rsd contribution.

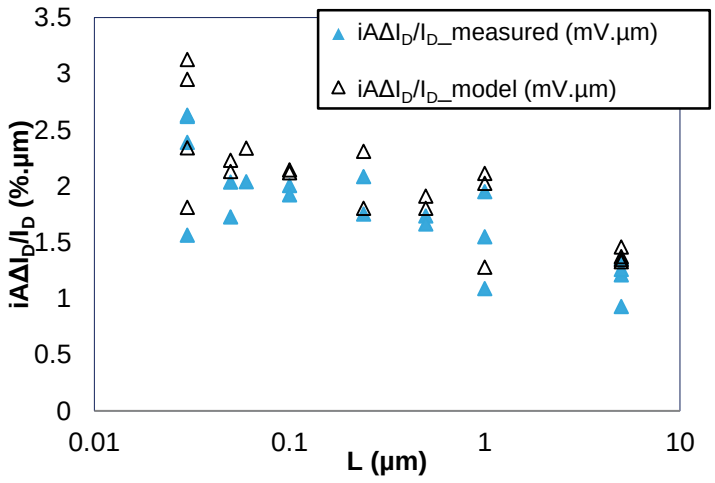


Figure IV. 23: Transistors with Pockets: Current variability from Croon's model compared to the measured current mismatch for transistors without Ge

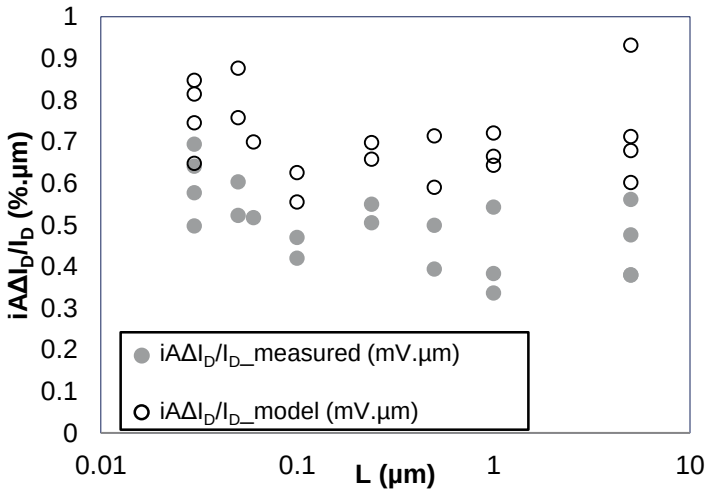


Figure IV. 24: Transistors with Pockets: Current variability from Croon's model compared to the measured current mismatch for transistors with 32-34% Ge

IV.5 Conclusions

This chapter presented a mismatch study performed on P-MOS transistors of advanced technology integrating High K/metal gate and SiGe channels. Vt, β and I_D mismatch have been studied in linear regime. Transistors with and without pocket implants, and comparisons between channels without Germanium and with different percentages of Germanium have been shown.

It was observed that for transistors without pockets, the Vt mismatch does not vary with the introduction of Ge, due to the negligible variability of the SiGe layer thickness (T_{SiGe}) and of the valence band offset (ΔEv). In contrast, for transistors with pocket implants, the Vt mismatch is shown to improve with the introduction of Ge. This improvement is attributed to the diffusion of the pocket dopants (type: Arsenic) in the channel, enlarging and dispersing the pockets and thus alleviating the contrast with the rest of the channel. Moreover, no Vt mismatch variation was observed with increasing Ge percentage.

Concerning the current gain factor, this study shows that the corresponding mismatch is improved with the introduction of Ge. This improvement is attributed to the reduction of the Coulomb scattering (charges at the $SiGe/SiO_2$ interface, defects or traps in the dielectric) with the introduction of Ge. This is the case for transistors with and without pocket implants. Moreover, the increased percentage of Ge does not induce any variation of current gain factor mismatch.

Finally, concerning the drain current mismatch, Croon's model has been found appropriate for transistors without pockets, with or without Ge. As the current mismatch is a combined result of the threshold voltage mismatch, the current gain factor mismatch and their correlation, any amelioration in one of these parameters induces a consequent current mismatch improvement. For transistors with pocket implants, Croon's model for current variability only offers a good fit for transistors without Ge, while it overestimates the measured values in the case of transistors with Ge. Thus, more variability sources should be considered, such as the source/drain series resistance Rsd, to better model the drain current mismatch, as explained in chapter II.

Chapter V

Mismatch characterization of 20nm Gate-last Bulk CMOS technology

This second technology chapter treats the metal gate granularity problem. Particular focus is given to the use of Gate-last technology to alleviate or completely remove the corresponding contribution to mismatch. For this purpose Vt and β mismatch for the 20nm Gate-last bulk CMOS technology are investigated and compared to 28nm Gate-first technology. Moreover, trends for $iA_{\Delta Vt}$ and $iA_{\Delta\beta/\beta}$ are analyzed as a function of EOT (Tox), from the 90nm technology node down to the 20nm technology node.

This chapter comprises the following six sections.

- Section I presents a general introduction on the problem of metal gate granularity (MGG). The state of the art with regards to the MGG effect on mismatch and to the use of Gate-last technology, known to theoretically reduce this contribution, is also presented.
- Section II describes some experimental details.
- Section III provides a comparison of the CMOS electrical parameters of GO1 and GO2 devices, which differ by different oxide thickness (for 20nm Gate-last technology).
- Section IV presents a comparison of the CMOS electrical parameters of 20nm Gate-last technology and 28 nm Gate first technology.
- Section V provides an analysis of the Vt and β mismatch constants as a function of EOT (Tox), from the 90nm technology node down to the 20nm technology node.
- Section VI concludes the chapter by drawing detailed conclusions and perspectives.

V.1 Introduction (State of the art)

Recent mismatch studies such as [Roy 06] [Cathignol 08b] [Asenov 08] [Wang 12] demonstrated that the main contributing factors to the threshold voltage (Vt) mismatch in advanced Bulk High-k / metal gate technology are the Random Dopant Fluctuations (RDF), the Line Edge Roughness (LER), and the Metal Gate Granularity (MGG).

The implantation and activation of self-aligned source and drain induces a poly-crystallization of the metal gate [Bai 05] [Fillot 05]. The grains so created have inconsistent orientation and work functions, and grow in size until reaching dimensions that are comparable to the gate length. This phenomenon is known as Metal Gate Granularity (MGG). One of the proposed solutions to eliminate the variability due to MGG is the use of Gate-Last technology, in which the metal gate is deposited after the implantation and the activation processes. The metal does not undergo high temperature treatments and maintains therefore its amorphous phase, with nanometer-scale grain sizes [Mistry 07] [Ohmori 08]. The adoption of Gate-Last technology in advanced bulk MOSFET's integrating High-k and metal gate is thus a promising solution that can help reduce the Vt mismatch.

Simulation studies by Asenov *et al*. [Asenov GSS] have been reported in literature on the advantages of Gate-Last technology in terms of reducing the Vt mismatch as compared to Gate-First technology. Moreover, a recent work by Fukutome *et al*. [Fukutome 12] showed that low Vt mismatch can be obtained for Gate-last technology by using embedded SiGe interface engineering, resulting in lower interface states density.

In this chapter the threshold voltage Vt, the current gain factor β, and the drain current I_D mismatch performances are investigated in the recent 20nm Gate-Last bulk CMOS technology. The values of Vt and β for this technology are also compared to those observed in the 28nm Gate-First Bulk technology. Finally, the trends of the Vt and β mismatch parameters across the nodes from 90nm ST technology down to 20nm Gate-Last technology are plotted and conclusions drawn.

V.2 Experimental details

Electrical characterization was performed on bulk NMOS/PMOS transistors on two wafers processed with 20nm Gate-Last International Semiconductor Development Alliance (ISDA) and 28nm Gate-First technologies, with integrated High-k gate oxide and metal gate.

The characteristics of the devices under test are detailed in Table V.1. For the 20nm Gate-Last technology, two equivalent gate oxide thicknesses are available (GO1 vs GO2). For matching measurements, a sample of 76 pairs of identical MOS transistors has been considered. The two MOSFET's of the pair are spaced by the minimum allowed distance, laid out in an identical environment and are electrically independent with symmetrical connections.

Table V. 1: Characteristics of the devices under test

	20 nm Gate-Last	28nm Gate-First
EOT (T_{ox})	GO1:12.48Å/12.7Å (NMOS/PMOS) GO2:31.6Å/32.9Å (NMOS/PMOS)	GO1:15.7Å/17.1Å (NMOS/PMOS) …….
High k	SiON/HFO2	HFSION
Metal Gate	- Based on TiN/TaN/Al (NMOS/PMOS)	- TiN / AO (NMOS) - TiN/AO/TiN/Al/TiN (PMOS)
PMOS transistors	Si channel	SiGe channel

The dimensions of the devices used in this study are detailed in Table V.2 for 20nm Gate-Last and 28nm Gate-First technologies.

Tests have been performed in linear regime with:

- Drain voltage $|V_D| = 0.05V$ and gate voltage $0 \leq |V_G| \leq 0.9V$ for 20nm GO1 devices;
- Drain voltage $|V_D| = 0.1V$ and gate voltage $0 \leq |V_G| \leq 1.8V$ for 20nm GO2 devices;
- Drain voltage $|V_D| = 0.05V$ and gate voltage $0 \leq |V_G| \leq 1V$ for 28nm GO1 devices;

All presented results refer to measurements performed at 25°C. In this work, samples of 76 pairs of MOS transistors are considered for each device type and wafer. The number of data rejects after filtering ranges between 0 and 5 in all wafers tested for this work. The filtered data is proven to follow a Gaussian distribution centered on 0.

The individual mismatch constant of Equation I.29 is used in this study with the purpose of evaluating the mismatch properties in the 20nm Gate-Last technology and comparing the performances with the 28nm Gate-First technology for each channel dimension.

Table V. 2: Dimensions of the devices under test for 20nm Gate-Last and 28nm Gate-First

28nm Gate-First GO1		20nm Gate-Last GO1		20nm Gate-Last GO2	
W (µm)	**L (µm)**	**W (µm)**	**L (µm)**	**W (µm)**	**L (µm)**
0.072	0.03	0.06	0.02	0.32	0.15
0.072	0.048	0.2	0.02	0.16	0.15
0.45	0.093	0.3	0.02	0.5	0.1
0.9	0.03	0.5	0.02	0.32	0.1
0.9	0.048	1	0.02	0.16	0.1
0.9	0.903	0.06	0.024	0.5	0.07
4.5	0.453	0.2	0.026	0.32	0.07
9	0.03	0.2	0.028	0.16	0.07
9	0.903	0.2	0.024	2	0.5
0.45	0.03	0.3	0.024	2	0.3
0.9	0.057	1	0.024	2	0.2
0.9	0.219	0.06	0.034	2	0.15
0.072	0.903	0.2	0.034	2	0.12
0.45	0.453	1	0.034	2	0.1
0.9	0.093	0.5	0.024	2	0.07
0.45	0.219	0.5	0.034	0.5	0.15
		1	0.06		
		0.5	0.06		
		1	0.08		
		0.5	0.08		
		1	1		
		0.5	1		
		0.5	2		

V.3 Comparison of devices with channel pocket implants and different oxide thicknesses EOT (Tox) in 20nm Gate-Last technology

The Vt, β, and I_D mismatch are analyzed in the 20nm Gate-Last technology by comparing GO1 and GO2 devices with different oxide thicknesses shown in Table V.1. This comparison enables a discussion on the possibility of reducing or eliminating the metal gate granularity effect in the 20nm Gate-Last technology.

V.3.1 Threshold Voltage mismatch

The Vt values were first measured using the maximum slope method [Hao 85], for GO1 and GO2 devices with thinner and thicker gate oxide, respectively. The results are plotted in

Figure V. 1 as a function of the gate length (L). NMOS GO2 devices exhibit higher |Vt| values compared to PMOS GO2 devices. Moreover, for GO2 PMOS devices a width (W) effect is observed. Indeed for the same gate length, when W is increased Vt is decreased. For example in Figure V. 1, for L=0.1µm, when W varies from 2µm to 0.16µm, the corresponding Vt values increase from 0.48V to 0.53V.

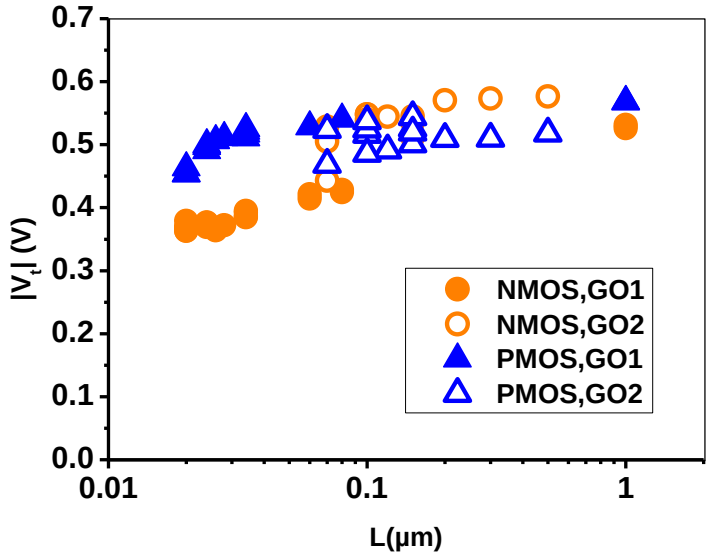


Figure V. 1: Comparison of |Vt| (V) as a function of the transistor surface W.L (µm^2) between GO1 and GO2 for NMOS and PMOS devices of the 20nm Gate-Last technology.

The values of $\sigma_{\Delta Vt}$ for GO1 and GO2 N/PMOS devices of 20nm Gate-Last technology are then calculated and plotted as a function of 1/W.L in Figure V. 2. This Graph shows that while GO1 N/PMOS transistors follow Pelgrom's Law except for very large areas, GO2 devices are much more dispersed. This higher dispersion may be due to process variations that might be not well controlled for GO2 devices. Future investigations should be devised to understand and quantify this phenomenon.

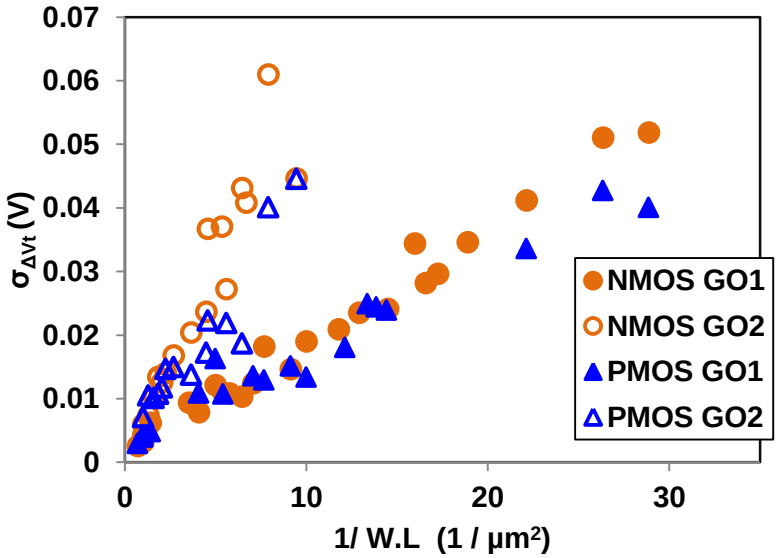


Figure V. 2: Pelgrom Plot: Comparison of $\sigma_{\Delta Vt}$ (V) as a function of the transistor surface 1/W.L (1/µm^2) between GO1 and GO2 for NMOS and PMOS devices of the 20nm Gate-Last technology.

The individual mismatch constant is then calculated using Equation I.29 for each geometry, and plotted as a function of the transistor surface W.L (µm^2) in Figure V. 3. The graph shows higher degradation of the $iA_{\Delta Vt}$ values in N/PMOS GO2 devices as compared to N/PMOS GO1 devices for different values of W.L (µm^2).

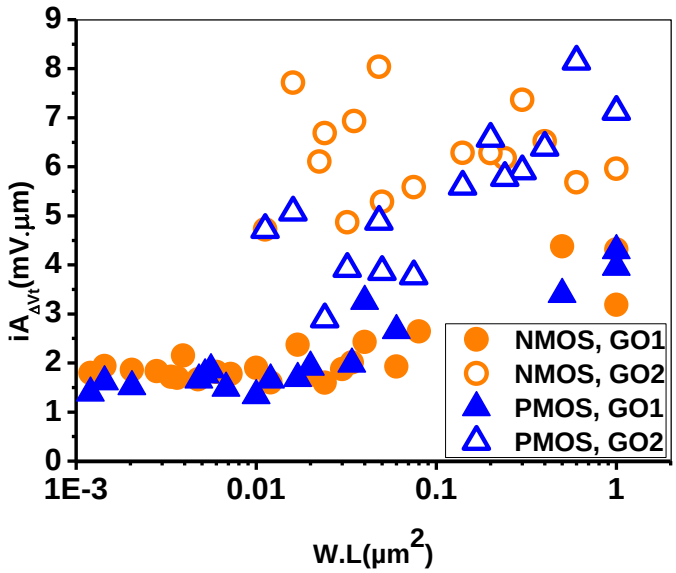


Figure V. 3: Comparison of $iA_{\Delta Vt}$ (mV.µm) as a function of the transistor surface W.L (µm^2) between GO1 and GO2 for NMOS and PMOS devices of the 20nm Gate-Last technology.

To explain the observed phenomenon, the effective channel doping (N_a) was extracted for long devices W=1µm/L=1µm (GO1) and W=2µm/L=0.5µm (GO2) using Equations V.1 and V.2, as detailed in [Ghibaudo 97], with the bulk bias shown in Table V.3:

$$\frac{dV_t}{dV_b} = -\frac{C_d}{C_{ox}} \qquad \textbf{(V.1)}$$

$$C_d(N_a) = \sqrt{\left(q.\varepsilon_{si}.N_a\right) \Big/ \left[4.K.T.\ln\left(\frac{N_a}{n_i}\right)\right]} \qquad \textbf{(V.2)}$$

where C_d is the channel depletion capacitance, C_{ox} is the oxide capacitance, ε_{si} is the channel permittivity, n_i is the intrinsic carrier concentration, K is the Boltzmann constant, and T is the measurement temperature in Kelvin.

Table V. 3: Bulk bias values used to extract the channel effective doping (N_a).

	GO1 devices (W=1µm/L=1µm)	**GO2 devices (W=2µm/L=0.5µm)**
NMOS	V_b=-0.5V & V_b=0V	V_b=-1V & V_b=0V
PMOS	V_b= 0.5V & V_b=0V	V_b=1V & V_b=0V

The obtained values for N_a, detailed in Table V.4, show very small difference between GO1 and GO2 devices.

Table V. 4: Effective channel doping in the 20nm Gate-Last technology.

	GO1 devices (W=1µm/L=1µm)	**GO2 devices (W=2µm/L=0.5µm)**
N_a NMOS	$1.21\text{x}10^{18}\text{cm}^{-3}$	$1.12\text{x}10^{18}\text{cm}^{-3}$
N_a PMOS	$1.90\text{x}10^{18}\text{cm}^{-3}$	$9.98\text{x}10^{17}\text{cm}^{-3}$

The individual mismatch parameter of the channel depletion charge Q_d was then calculated using Equation V.3 in order to normalize the Vt mismatch and eliminate the T_{ox} dependency.

$$\sigma_{\Delta Qd} = \mathrm{Cox}.\sigma_{\Delta \mathrm{Vt}} \qquad \textbf{(V.3)}$$

The results, plotted in Figure V. 4 as a function of W.L (μm^2), interestingly show that N/PMOS GO1 and GO2 devices exhibit comparable $iA_{\Delta Qd}$ values over the studied range of W.L. This similarity suggests that the Vt mismatch scales with T_{ox} and further indicates, based on Equation V.4 [Mezzomo 10], that in the 20nm Gate-last technology the channel contribution to the Vt mismatch is much more pronounced than the gate contribution.

$$A_{Vt}(t_{ox}) = \sqrt{\frac{t_{ox}^{\ 2}}{\varepsilon_{ox}^{\ 2}} \cdot \frac{q.Q_d}{4}} \qquad \textbf{(V.4)}$$

where ε_{ox} is the oxide permittivity.

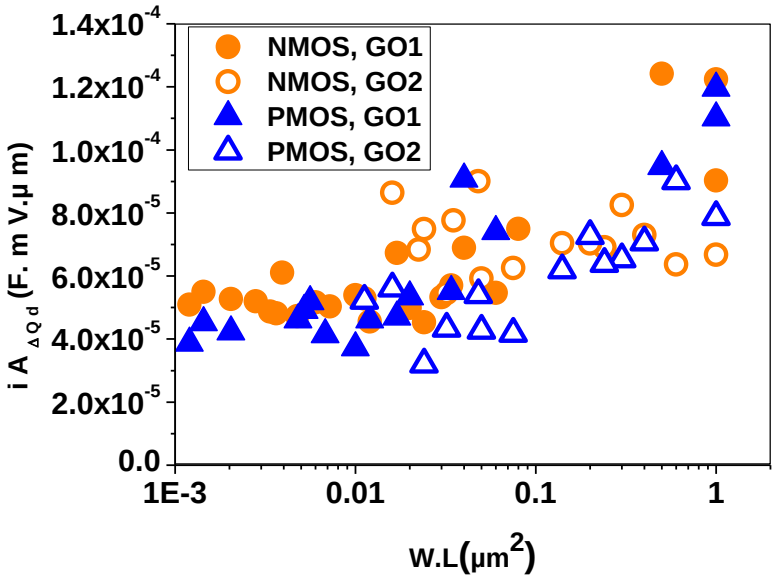


Figure V. 4: Comparison of $iA_{\Delta Qd}$ (F.mV.µm) as a function of W.L (μm^2) between GO1 and GO2 for NMOS and PMOS devices of the 20nm Gate-Last technology.

The two previous conclusions demonstrate that by using a Gate-Last technology and thus improving the MGG effect, the gate contribution to the Vt mismatch can be effectively eliminated.

V.3.2 Current gain factor mismatch

The current gain factor (β) was also extracted using the maximum slope method [Hao 85]. The β individual constant of mismatch was then calculated using Equation I.29 for each transistor geometry. The results are plotted in Figure V. 5, indicating that both N/P MOS GO1 devices exhibit significant improvement and lower β mismatch dispersion as compared to GO2 transistors.

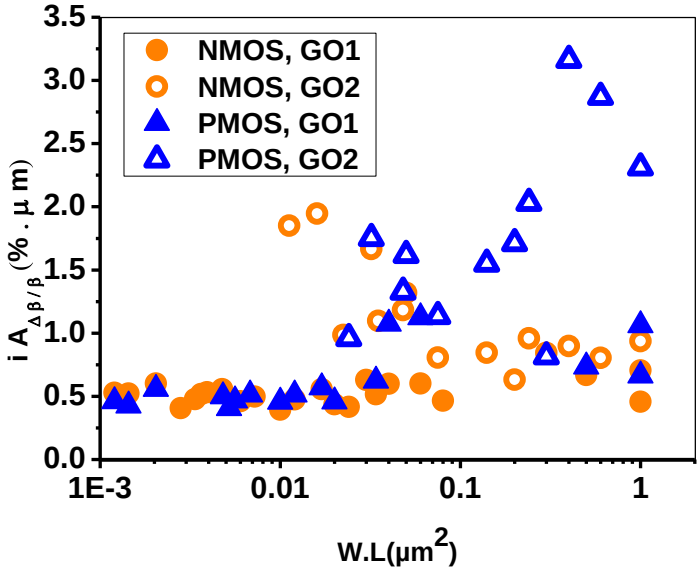


Figure V. 5: Comparison of $iA_{\Delta\beta/\beta}$ (%.µm) as a function of the transistor surface W.L (µm²) between GO1 and GO2 for NMOS and PMOS devices of the 20nm Gate-Last technology.

V.3.3 Drain Current mismatch

The drain current mismatch was finally investigated in GO1 and GO2 devices. The drain current was measured in linear regime with $|V_D|$=0.05V and $|V_G|$=0.9V for GO1 (N/P) devices and $|V_D|$=0.1V and $|V_G|$=1.8V for GO2 devices. The individual constant of mismatch was then calculated using Equation I.29 and the results plotted in Figure V. 6.

The graph of Figure V. 6 shows that for small devices (W.L <0.1 µm²) no significant variation is observed between GO1 and GO2 N/P MOS transistor devices. The values for GO1 and GO2 PMOS devices are however very dispersed. For larger dimensions (W.L ≥ 0.1 µm²), GO1 exhibit degraded mismatch values as compared to GO2 devices for NMOS transistors and improved mismatch values for PMOS transistors. For large areas, GO1 and GO2 PMOS devices are also more dispersed.

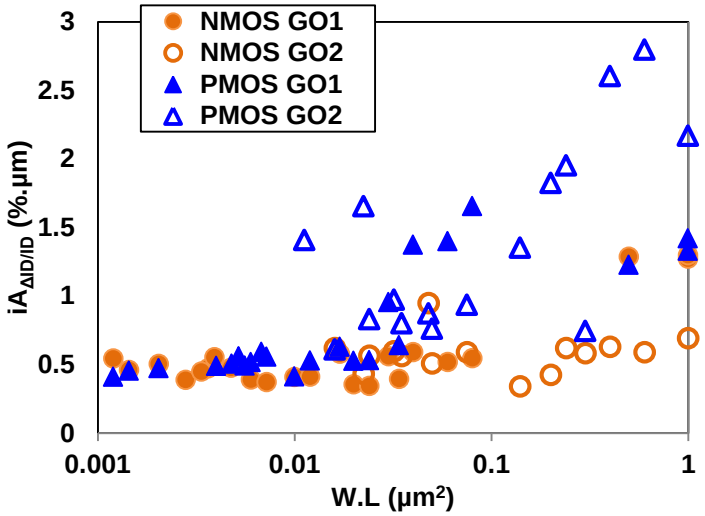


Figure V. 6: Comparison of $iA_{\Delta ID/ID}$ (%.µm) as a function of the transistor surface W.L (µm²) between GO1 and GO2 for NMOS and PMOS devices of the 20nm Gate-Last technology.

To understand the phenomenon observed in the measurement data for I_D mismatch, the Croon model in [Croon 02] expressed by Equation III.1 and the improved Croon model [Rahhal 13] derived in III.2 were plotted for GO1 and GO2 NMOS transistors in Figure V. 7.a and Figure V. 7.b respectively.

Figure V. 7.a shows that the Croon model and the improved Croon model reproduce the measured I_D mismatch data, indicating that the R_{sd} contribution to the I_D mismatch is negligible in GO1 devices. The graph also shows that, for W.L $\leq 0.1\mu m^2$, the β mismatch term is more pronounced than the Vt mismatch term, dominating the I_D mismatch as a function of W.L. As for W.L > $0.1\mu m^2$, the Vt mismatch term is more pronounced than the β mismatch term, dominating the I_D mismatch as a function of W.L. As for GO2 devices, Figure V. 7.b shows that while the Croon model in Equation III.1 does not fit the measured data, the improved Croon model in Equation III.2 better describes the experimental trend. This indicates that the R_{sd} contribution is an important factor in the I_D mismatch across the whole range of W.L. Figure V. 7.b also shows that the β mismatch term dominates the I_D mismatch across the whole range of W.L. Similar results were obtained for PMOS devices.

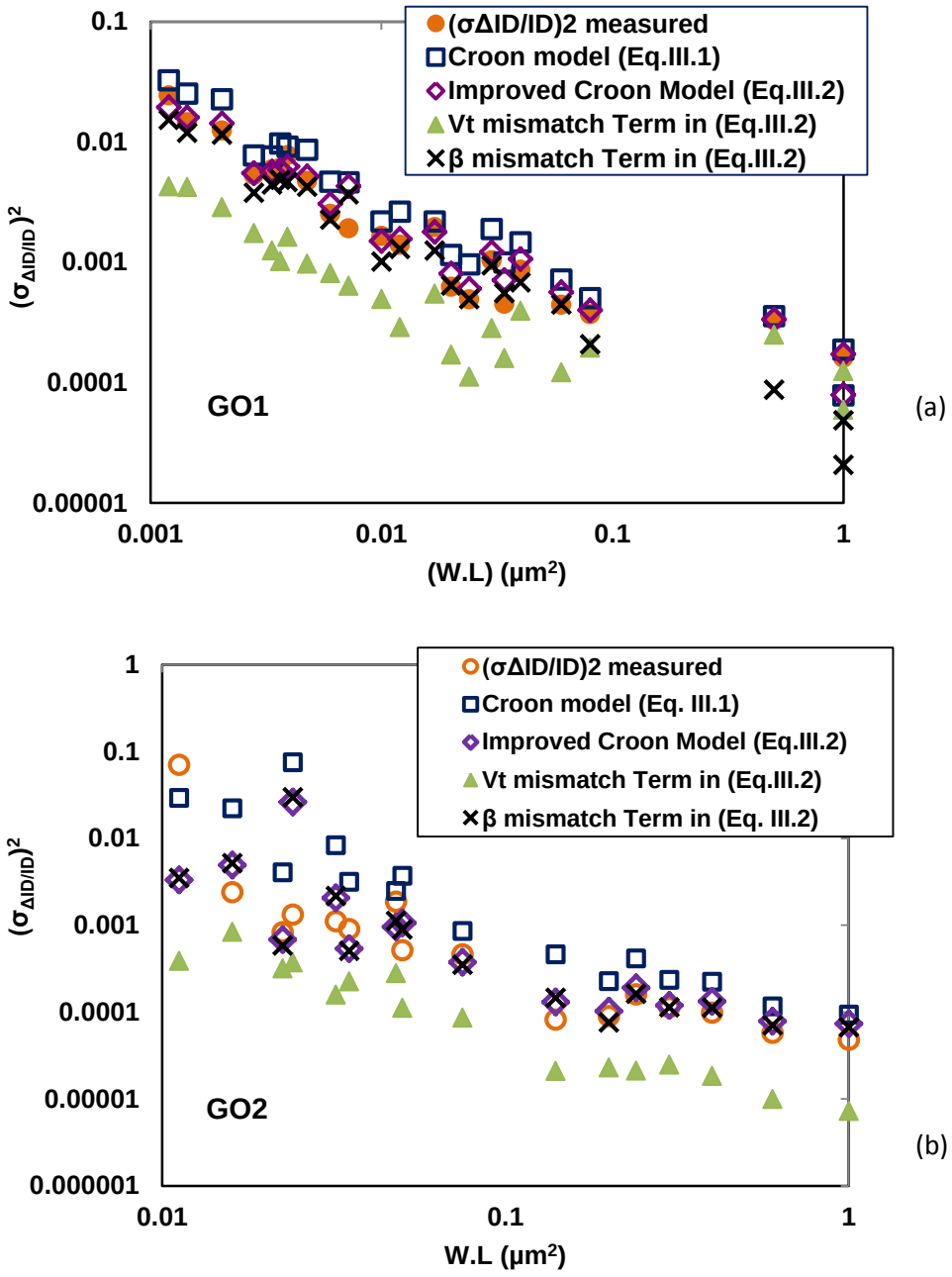


Figure V. 7: 20nm Gate-last technology: Measured $\sigma_{\Delta ID/ID}$, Croon's model & improved Croon Model as a function of the transistor surface W.L (μm^2) for (a) GO1 and (b) GO2 NMOS devices.

The presented results show that the improved Croon Model better reproduces the measured I_D mismatch for all devices (GO1/GO2 and N/P MOS) and that the R_{sd} contribution is significant in GO2, but negligible in GO1 devices.

The last investigation conducted in this study is focused on the $\left|G_m/I_D\right|$ contribution to the Vt mismatch term in Equation III.2. This parameter is plotted in Figure V. 8 for the whole range of W.L. The graph shows a significant gap between the $\left|G_m/I_D\right|$ values of GO1 and

GO2 devices. Moreover, the trend of $|G_m/I_D|$ as a function of W.L is very similar to that observed for $iA_{\Delta ID/ID}$ in Figure V. 6. This suggests that, while the Vt and β mismatch are considerably degraded in GO2 devices as compared to GO1 devices, the I_D mismatch measurements on the two devices exhibit smaller differences due to the R_{sd} contribution and the $|G_m/I_D|$ gap.

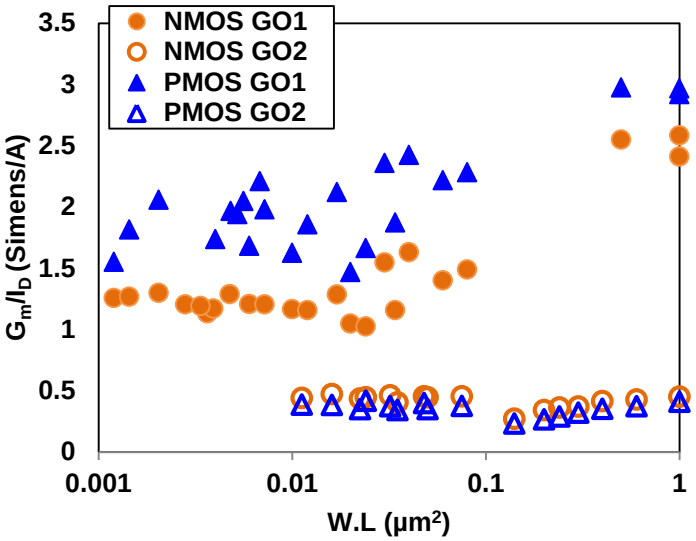


Figure V. 8: Comparison of G_m/I_D (Simens/A) as a function of the transistor surface W.L (μm^2) between GO1 and GO2 for NMOS and PMOS devices of the 20nm Gate-Last technology.

V.4 Comparison between 28nm Gate-first and 20 nm Gate-last Bulk technologies

After demonstrating that the MGG effect is effectively eliminated in the 20nm Gate-Last technology, a comparison between this technology and the previous 28nm Gate-First technology is proposed. Note that, for both technologies, this study considers GO1 devices with pocket implants and thin, yet different oxide thicknesses.

V.4.1 Threshold Voltage mismatch

The Vt values were first measured using the maximum slope method [Hao 85] for 20nm Gate-Last and 28 Gate-First GO1 devices. The results are plotted in Figure V. 9 as a function of the gate length (L), showing that N/P MOS devices of the 28nm technology exhibit reverse

short channel effects across the whole range of L, while 20nm Gate-last devices are affected by smaller Vt variations as a function of L and less significant short channel effects for L<0.06µm. Note that both 20nm and 28nm technologies present pocket implants in the channel. A width effect is also observed for 28nm NMOS Gate-First technology. At a given gate length, when W increases, Vt decreases. For example in Figure V.9, for L=0.0.3µm, when W decreases from 10µm to 0.08µm, the corresponding Vt values increase from 0.34V to 0.55V.

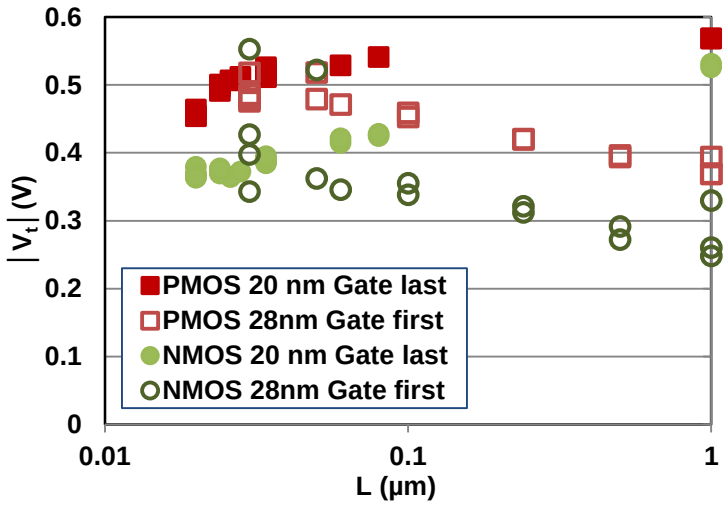


Figure V. 9: Comparison of |Vt| (V) as a function of L (µm) between NMOS and PMOS devices of the 28nm Gate-First and 20nm Gate-Last technologies.

The individual Vt mismatch parameter is thus calculated from the Vt values for 20nm and 28nm technologies and plotted in Figure V. 10 as a function of L(µm). For nominal devices, very promising $iA_{\Delta Vt}$ values of 1.79mV.µm and 1.3mV.µm are observed for N and P MOS devices, respectively. Furthermore, Figure V. 10 shows that, for short devices where the pockets are close one to another, 20nm Gate-Last devices presents improved $iA_{\Delta Vt}$ values as compared to 28nm Gate-First devices for both N and P MOS transistors.

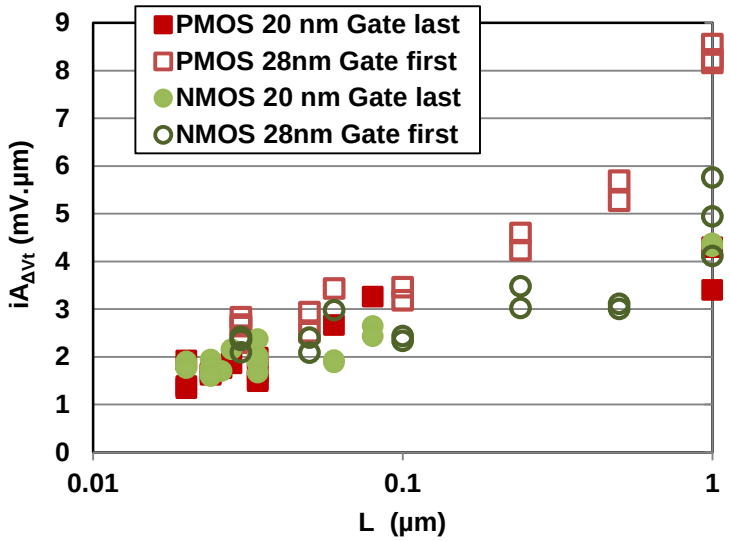


Figure V. 10: Comparison of $iA_{\Delta Vt}$ (mV.µm) as a function of L (µm) between NMOS and PMOS devices of the 28nm Gate-First and 20nm Gate-Last technologies.

As for long devices, the 20nm technology shows smaller hump at L=1µm. Note that the improvement of $iA_{\Delta Vt}$ over the whole range of L is more pronounced for PMOS devices. For long devices, the effective channel doping (N_a) was extracted for W=1µm/L=1µm using Equations V.1 and V.2, where Vt was obtained for bulk bias values as shown in Table V.3. The extracted values of N_a are detailed in Table V.5.

Table V. 5: Effective channel doping in the 20nm Gate-Last and 28 nm Gate-first technologies.

W=1µm/L=1µm	20 nm Gate-last	28nm Gate-first
N_a NMOS	$1.21x10^{18}cm^{-3}$	$1.98x10^{17}cm^{-3}$
N_a PMOS	$1.90x10^{18}cm^{-3}$	$1.65x10^{17}cm^{-3}$

Mezzomo *et al*. demonstrated that higher levels of pocket doping induce mismatch degradation in both short and long transistors, and that long transistors are additionally affected by larger Vt mismatch as the contrast between the doping level in the pockets and in the rest of the channel increases [Mezzomo 10]. With regard to the mismatch data, this suggests that the pocket implants in 20nm Gate-First devices are less doped compared to 28nm Gate-Last devices. As for long devices, Table V.4 shows that N_a is higher in 20nm

Gate-Last devices compared to 28nm Gate-First devices, suggesting that the contrast between the pockets and the rest of the channel is less pronounced in the 20nm node than in the 28nm node as illustrated in Figure V. 11. The combined contrast of pockets and channel doping induces the observed improvement in Vt mismatch and the smaller hump for lengths approaching L=1µm.

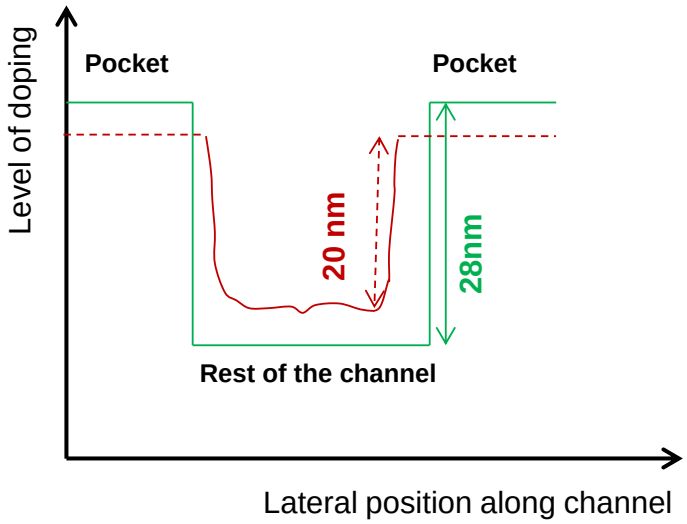


Figure V. 11: Schematic illustration of the contrast between the pocket doping and the rest of the channel for 20nm Gate-last technology and 28nm Gate first technology.

V.4.2 Current gain factor mismatch

The current gain factor (β) was also extracted using the maximum slope method [Hao 85]. The β individual constant of mismatch was then calculated using Equation I.29 for each transistor geometry and the results are plotted in Figure V. 12. This graph shows that the 20nm technology exhibits significant improvement and less dispersion of the β mismatch values as compared to 28nm technology for both N and P MOS devices.

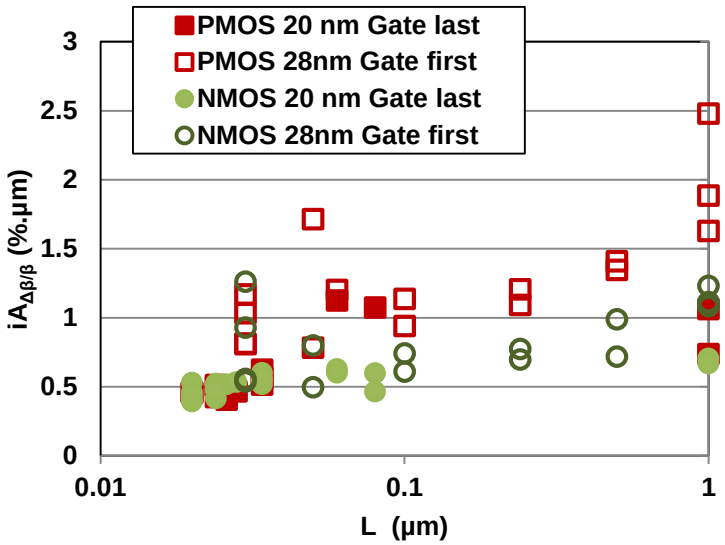


Figure V. 12: Comparison of $iA_{\Delta\beta/\beta}$ (%.µm) as a function of L (µm) between NMOS and PMOS devices of the 28nm Gate-First and 20nm Gate-Last technologies.

V.5 Vt and β mismatch trends as a function of Tox

The benchmark plot of Figure V. 13 illustrates the trend of $iA_{\Delta Vt}$ for NMOS and PMOS transistors from the 90nm ST node down to the 20nm Gate-Last ISDA node, as a function of T_{ox} (EOT). The graph shows that the linear trends of $iA_{\Delta Vt}$ for older technologies until the 45nm Poly-Gate node have a non-zero offset (y-axis intercept). Asenov *et al*. showed that such offset is directly related to the material-Gate contribution, which does not scale with T_{ox} and approaches zero starting from the 28nm Metal Gate technology [Asenov 00]. This suggests that the gate mismatch contribution is negligible compared to the channel contribution. This phenomenon is more pronounced in the 20nm Gate-Last technology, exhibiting large $iA_{\Delta Vt}$ improvement for thin T_{ox}. The Gate-last technology therefore enables a reduction of the MGG contribution to the Vt mismatch, and the gap between 28nm Gate First and 20nm Gate-Last technologies is of 0.5 mV.µm, corresponding to $iA_{\Delta Vt}$ values of 2.4mV.µm for 28nm Gate-First and 1.9 mV.µm for 20nm Gate-Last. Note that the values of $iA_{\Delta Vt}$ were calculated using Pelgrom's law, where $iA_{\Delta Vt}$ is constant for varying L. The same conclusions were also drawn for PMOS devices from Figure V. 13.b, which indicates a higher gap of 0.9mV.µm between the 28nm Gate-First and the 20nm Gate-Last technologies.

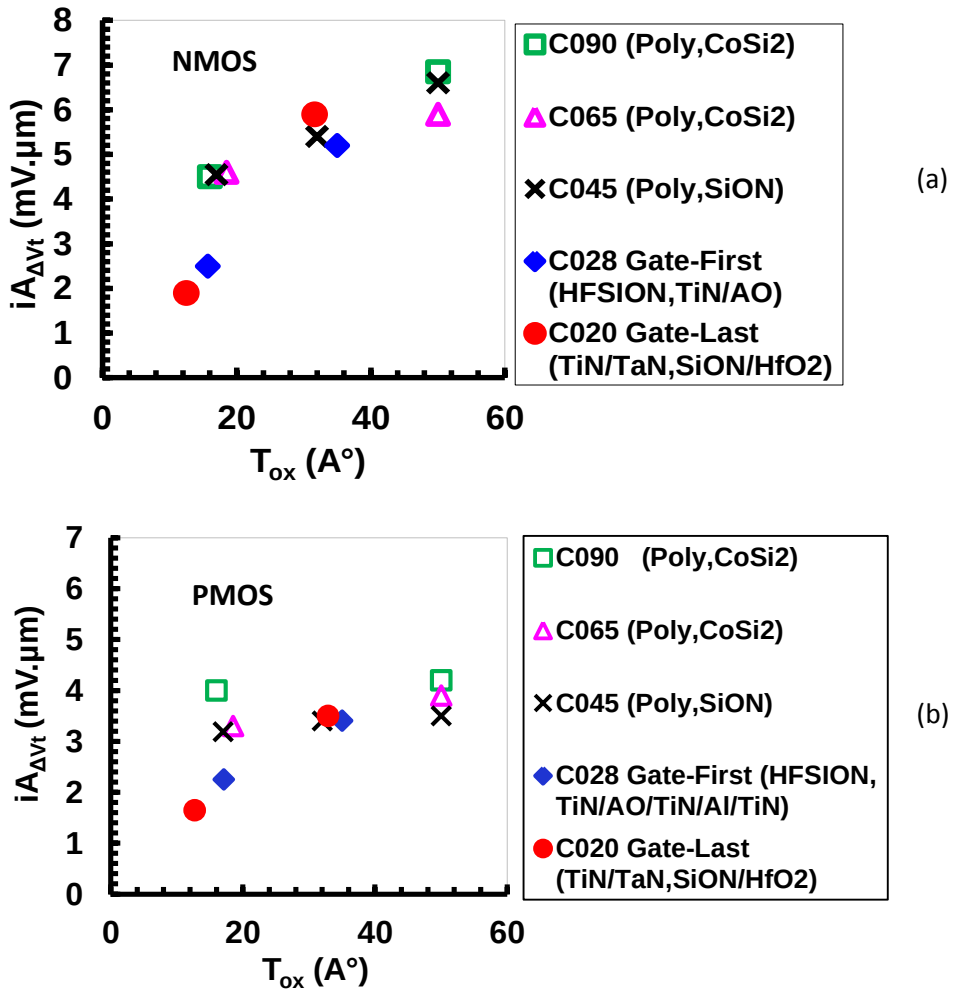


Figure V. 13: Trend of $iA_{\Delta Vt}$ (mV.µm) as a function of the oxide thickness T_{ox} (Å) from 90nm ST Bulk technology to 20nm Gate-Last Bulk technology (a) for NMOS devices and (b) for PMOS devices.

Similarly, for the β mismatch the values of $iA_{\Delta\beta/\beta}$ were calculated using Pelgrom's law, since $iA_{\Delta Vt}$ is a constant with respect to variations of L. The $iA_{\Delta\beta/\beta}$ parameter for NMOS transistors was plotted as a function of T_{ox} (EOT) for the nodes from 90nm ST bulk technology to the 20nm Gate-Last ISDA node. The corresponding graph, shown in Figure V. 14.a, does not indicate any specific variation as a function of T_{ox} or technology-dependent trend. Note that GO1 devices (NMOS/PMOS) of the 20nm Gate-Last technology exhibit improved β mismatch as a function of T_{ox}. However, for thick T_{ox}, the β mismatch value is comparable to the older ST technologies. The same conclusions were also drawn for PMOS devices from Figure V. 14.b. In this case, however, the values of $iA_{\Delta\beta/\beta}$ for the 20nm Gate

Last-technology are comparable to those measured for the other technologies and do not exhibit significant improvement.

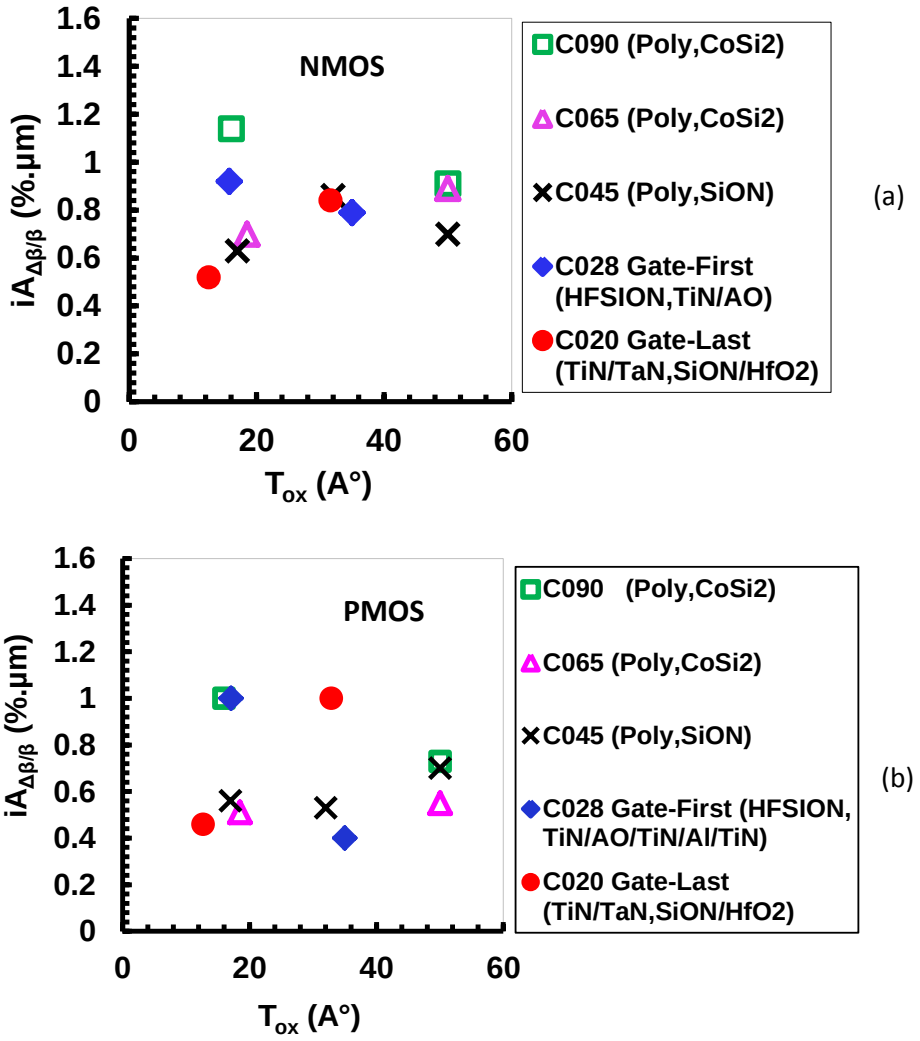


Figure V. 14: Trend of $iA_{\Delta\beta/\beta}$ (%.µm) as a function of the oxide thickness T_{ox} (Å) from 90nm ST Bulk technology to 20nm Gate-Last Bulk technology (a) for NMOS devices and (b) for PMOS devices.

V.6 Conclusions

This chapter reports a study of the Vt, β, and I_D mismatch trends in 20nm Gate-Last bulk technology and presents a comparison with the previous 28nm Gate-First bulk technology. The results obtained from the comparison between GO1 and GO2 devices of the 20nm Gate-Last technology reveal superior Vt and β mismatch performance in thinner gate oxide (GO1) devices due to the larger gate coupling. As for the I_D mismatch, similar results were observed in GO1 and GO2, N/P MOS devices. This similarity was explained by fitting

the experimental data with the improved Croon model [22], which reproduces the measurement data and proves that the observed trend is a direct consequence of the R_{sd} and $\left|G_m/I_D\right|$ contributions.

With regard to the channel depletion charge (Q_d) mismatch, GO1 and GO2 devices exhibit identical $iA_{\Delta Qd}$ values. This similarity suggests that the Vt mismatch scales with T_{ox} and that the channel contribution to the Vt mismatch is more prominent than the gate contribution. By introducing improvements in the MGG effect, the Gate-Last technology enables the gate contribution to the Vt mismatch to be eliminated. Furthermore, the presented comparison between the 20nm Gate-First and 28 nm Gate-Last technologies shows that the former benefits from improved Vt and β mismatch performance.

Finally, the trends of Vt and β mismatch as a function of T_{ox} were plotted for the nodes from 90nm ST technology to 20nm Gate-Last ISDA technology. $iA_{\Delta\beta/\beta}$ does not exhibit any specific trend, neither as a function of T_{ox} nor over the different technologies. $iA_{\Delta Vt}$ shows a linear trend as a function of T_{ox} with an offset greater than zero for all nodes until the 45nm Poly-gate technology. Such offset approaches zero when moving from the 28nm Metal Gate technology to the 20nm Gate-Last technology, confirming that the MGG-induced mismatch is negligible. This also confirms that, for 28nm Metal Gate technology and 20nm Gate-Last technology, the principal contributing factor to the Vt mismatch remains the channel doping.

Chapter VI

Mismatch behavior in advanced FD SOI CMOS technologies

This chapter presents an exhaustive study of the mismatch behavior in advanced FD SOI technologies and it is divided into the following four sections.

- Section I presents a general introduction of FDSOI technology.
- Section II analyses the mismatch behavior and contributions in 14nm FDSOI technology. For this purpose, two devices (GO1 and GO2) with different oxide thicknesses are considered. The mismatch trends of Vt, β, and I_D are measured, compared and analyzed. The mismatch of these electrical parameters is further compared to the 28nm FD SOI technology, and conclusions are deduced.
- Section III provides an exhaustive study of Vt, β, and I_D mismatch behavior with transistor aging using NBTI stress tests. This study is performed on 28nm FD SOI technology, for which some models are presented and conclusions drawn.
- Section IV closes the chapter by identifying detailed conclusions.

VI.1 Introduction

Fully Depleted Silicon On Insulator (FD SOI) technology is considered as one of the best candidates to maintain consistency with the scaling law [Planes 12], [Arnaud 12]. Many studies have been conducted on advanced FD SOI transistors, showing that the FD SOI technology exhibits better Short Channel Effects (SCEs) than bulk technology, due to the thin film and undoped channel [Gallon 07]. Moreover, the use of ultra-thin body and buried oxide thickness (UTBB) offers enhanced scalability for the technology and provides an ideal sub-threshold slope and a better drain-induced barrier lowering (DIBL) [Gallon 07] [Barral 06]. Finally, the large back-to-front gate coupling provides good control of the Vt [Gallon 07] [Fenouillet-Beranger 08].

Many studies have demonstrated the better mismatch performance of the FD SOI technology compared with the Bulk technology, thanks to the mid-gap/high-k metal gate stack and the un-doped SOI films. A detailed report on the state of the art in SOI mismatch is presented in chapter I (section I.7.2).

All these studies were conducted on transistors at the beginning of their life (transistors aging time = 0). An unknown investigation is therefore herein considered: the mismatch behavior as a function of transistor aging (transistors aging time ≠ 0). Do the two FD SOI transistors of the pair age the same way? Does this have a direct impact on the stochastic mismatch? How does this mismatch behave as a function of time? How does it behave as a function of stress conditions?

In literature, most transistor aging mismatch studies were performed with using Bias Temperature Instability (BTI) Stress conditions. Indeed many studies such as [Rauch 07], [Huard 08], [Kaczer 10] and [Angot 13] observed the mismatch of the electrical parameter drift in two identical MOS transistors with the aim of quantifying the effects of aging differences within the pair. However, few studies were performed on the stochastic mismatch behavior as a function of time.

In this chapter, the two following major FD SOI aspects are considered.

- The mismatch performance of Vt, β and I_D for the 14nm and 28nm FD SOI technology at zero transistor aging time. A comparison between 14 nm and 28nm FD SOI technologies is proposed and conclusions are drawn in regards to the main electrical parameter mismatch contributions in FD SOI technology.
- The Vt, β and I_D mismatch behavior of 28 nm FD SOI technology as a function transistors aging. For this purpose, a Negative-Bias Temperature Instability (NBTI) stress is applied on GO1 and GO2 PMOS devices. The mismatch behavior of Vt, β and I_D is explored as a function of the drift of the considered parameters. The parameter drift illustrates the number of traps and defects added in the Si/SiO_2 interface as a function of time. Thus, some explanations and conclusions of Vt, β and I_D mismatch behavior as a function of the parameter drifts are drawn.

VI.2 Mismatch behavior in 14nm and 28 nm FD SOI CMOS technology

VI.2.1 Experimental details

Electrical characterization of bulk NMOS/PMOS transistors was performed on two wafers processed with 28nm and 14nm FD SOI technologies. The features of the devices under test are detailed in Table VI.1. For mismatch measurements, a sample of 76 pairs of identical MOS transistors has been considered. The two MOSFET's of the pair are spaced by the minimum allowed distance, laid out in an identical environment and are electrically independent, organised in the mismatch test structures detailed in Section I.5.2. Tests have been performed in linear regime with drain voltage $|V_D| = 0.05V$ for GO1 devices and $|V_D| = 0.1V$ for GO2 devices. The gate voltage $|V_G|$ ranges from 0 to 1V for 28nm and from 0 to 0.9V for 14nm GO1 devices. For GO2 devices, the gate voltage $|V_G|$ ranges from 0 to 1.8V for 28nm and 14nm GO2 devices. All the presented results refer to measurements performed at 25°C. In this work, the individual mismatch constant of Equation I.29 is considered. This parameter allows the evaluation of the mismatch values for each channel dimension (Section I.4.5.c).

Table VI. 1: Features of the Devices under Test

	28 nm FD SOI NMOS	**28 nm FD SOI PMOS**	**14 nm FD SOI NMOS**	**14 nm FD SOI PMOS**
EOT (Tox)	GO1: 15.5Å GO2: 34 Å	GO1: 17.5Å GO2: 35 Å	GO1: 13 Å GO2: 35 Å	GO1: 14.5Å GO2: 35 Å
Film Thickness (Tsi)	GO1: 7nm GO2: 7nm	GO1: 7nm GO2: 7nm	GO1: 5nm GO2: 5nm	GO1: 5nm GO2: 5nm
BOX thickness (T_{BOX})	GO1: 25 nm GO2: 25 nm	GO1: 25 nm GO2: 25 nm	GO1: 20nm GO2: 20nm	GO1: 20nm GO2: 20nm
High k/ Metal Gate	GO1: SiON/HfSiOn/TiN GO2: HTO/ SiON/HfSiOn/TiN	GO1: SiON/HfSiON/TiN GO2: HTO/ SiON/HfSiOn/TiN	GO1: SiON/HfO2N/TiN GO2: HTO/SiON/HfO2 N/TiN	GO1: SiON/HfO2N/TiN GO2: HTO/SiON/HfO2 N/TiN
Ge in the channel	GO1: w/o Ge GO2: w/o Ge	GO1: w/o Ge GO2: w/o Ge	GO1: w/o Ge GO2: w/o Ge	GO1: with Ge GO2: with Ge
S/D Types	GO1: w/o Ge GO2: w/o Ge	GO1: w/o Ge GO2: w/o Ge	GO1: w/o Ge GO2: w/o Ge	GO1: with Ge GO2: with Ge

VI.2.2 Effect of EOT: Comparison between GO1 and GO2 for 14nm FD SOI technology

The Vt, β and I_D mismatch are analyzed for 14 nm FDSOI technology by comparing GO1 and GO2 devices, which differ in oxide thickness. The effect of the oxide thickness on the mismatch trends in FD SOI technology is then discussed.

VI.2.2.a Threshold Voltage mismatch

The Vt values were first measured using the maximum slope method [Hao 85], for GO1 and GO2 devices with thinner and thicker gate oxide, respectively. Results are plotted in Figure VI. 1 as a function of the gate length (L). NMOS GO1 and GO2 devices exhibit identical Vt values. As for PMOS devices, GO1 transistors also exhibit values similar to those observed for NMOS GO1/GO2 transistors, which are lower than those measured for PMOS GO2 devices. The experiment also shows that short channel effects become evident in GO1 N/P MOS devices for L<0.06µm.

The individual mismatch constant (Equation I.29) is then calculated for each geometry, and plotted as a function of the transistor surface W.L (μm^2) in Figure VI. 2. This plot does not show significant differences between NMOS and PMOS transistors with thinner and thicker oxide, and further indicates that the Vt mismatch does not scale with Tox, as opposed to what seen in Bulk technology (see chapter V). The results also show that NMOS transistors exhibit better Vt mismatch performance compared to PMOS transistors. This difference can be due to process variations between NMOS and PMOS devices such as Ge additional processes. Soussou *et al.* in [Soussou 12] showed that when T_{SiGe} > 5nm in FD SOI devices, Vt variations are negligible. However when T_{SiGe} < 5nm Vt variations become noticeable, introducing a significant source of variability. In our case, a T_{SiGe} of 5nm is considered, and this might be one of the reasons for the mismatch degradation observed in the case of PMOS devices.

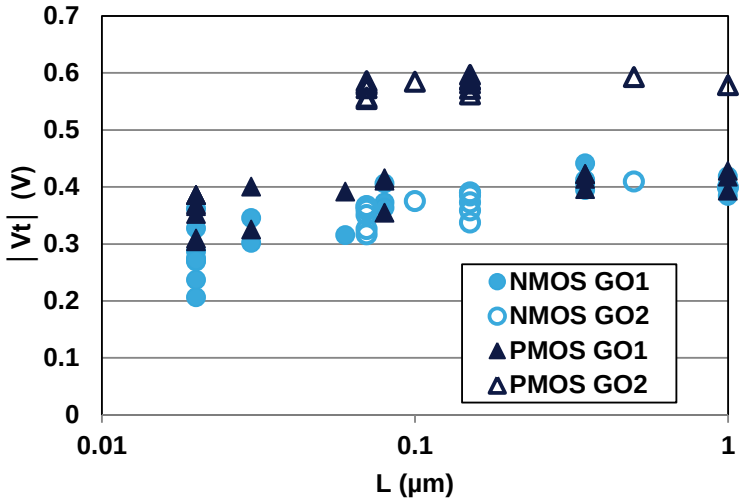


Figure VI. 1: Comparison of |Vt| (V) as a function of the transistor length L (µm) between GO1 and GO2 for NMOS and PMOS devices of 14nm FD SOI technology.

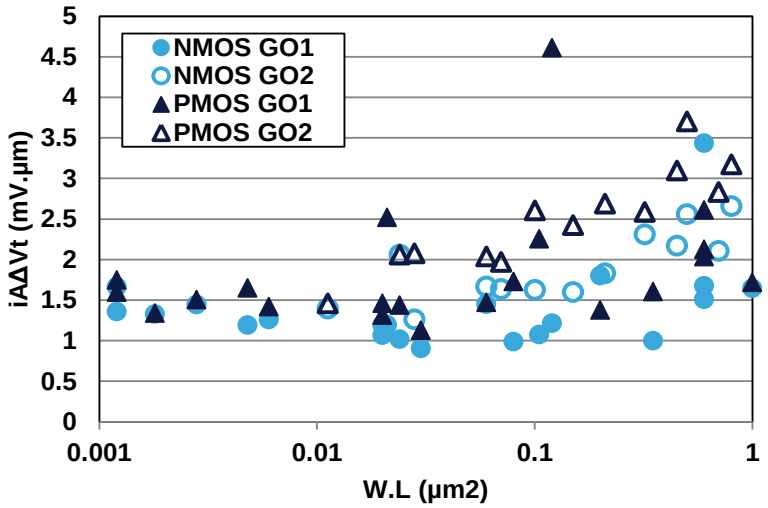


Figure VI. 2: Comparison of $iA_{\Delta Vt}$ (mV.µm) as a function of the transistor surface W.L (µm^2) between GO1 and GO2 for NMOS and PMOS devices of 14nm FD SOI technology.

VI.2.2.b Current gain factor mismatch

The current gain factor (β) was also extracted using the maximum slope method presented in [Hao 85]. The β individual constant of mismatch was then calculated using Equation I.29 for each transistor geometry and the results are plotted in Figure VI. 3. The graph indicates that GO1 and GO2 devices do not exhibit any significant difference and shows that the parameter $iA_{\Delta\beta/\beta}$ assumes lower values for NMOS devices compared to PMOS devices. This difference can be due to the presence of Ge in the channel and in the S/D or to the differences in the NMOS and PMOS lithography processes.

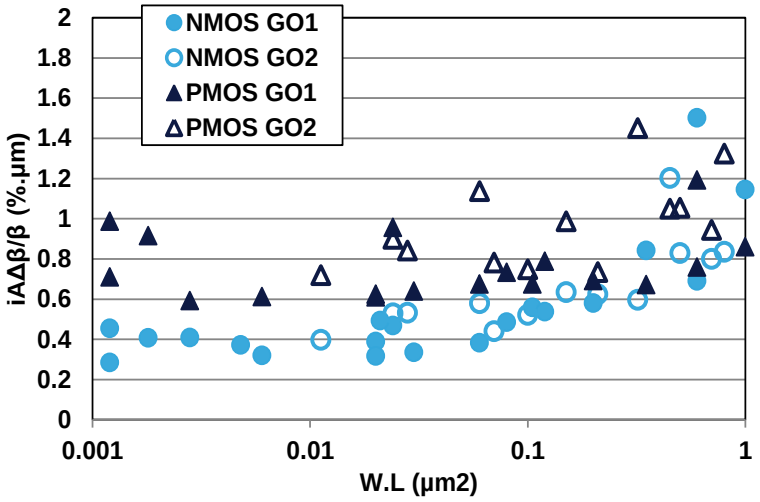


Figure VI. 3: Comparison of $iA_{\Delta\beta/\beta}$ (%.µm) as a function of the transistor surface W.L (µm^2) between GO1 and GO2 for NMOS and PMOS devices of 14nm FD SOI technology.

VI.2.3.c Drain current mismatch

The drain current mismatch was also investigated for GO1 and GO2 devices. The drain current was measured in linear regime with V_D=0.05V for GO1 devices and V_D=0.1V for GO2 devices. The individual constants of mismatch were then calculated using Equation I.29 and the results are plotted in Figure VI. 4. The graph does not show any significant difference between GO1 and GO2 devices, with PMOS transistors exhibiting higher drain current mismatch compared to NMOS transistors.

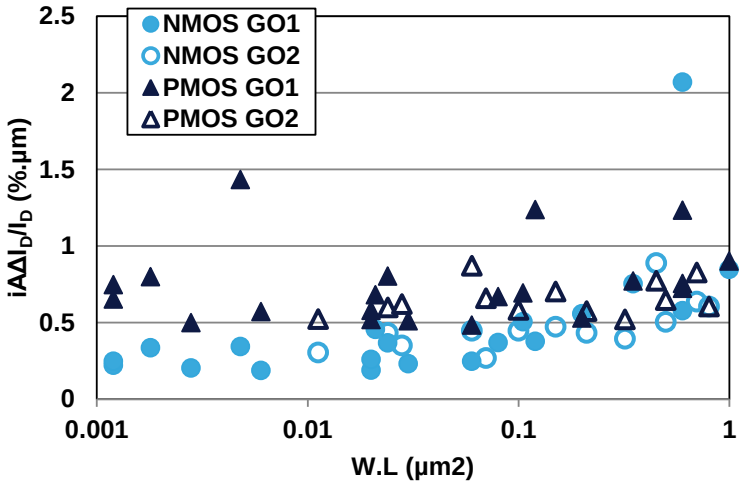


Figure VI. 4: Comparison of $iA_{\Delta I_D/I_D}$ (%.µm) as a function of the transistor surface W.L (µm^2) between GO1 and GO2 for NMOS and PMOS devices of 14nm FD SOI technology.

With the aim of gaining a better understanding of the observed drain current mismatch phenomena, two plots were produced that superimpose the measured I_D mismatch. These plots are Croon's model (Equation III.1) and the improved Croon model (Equation III.2) for GO1 and GO2 NMOS transistors, as shown in Figure VI. 5.a and Figure VI. 5.b, respectively.

Figure VI. 5.a indicates a small deviation between the plot of Croon's model and the measured data, whereas the improved Croon model offers a better fit. This indicates that the Rsd contribution is not negligible in the I_D mismatch for GO1 devices and that the Vt and β mismatch terms dominate the I_D mismatch as a function of W.L.

As for GO2 devices, Figure VI. 5.b indicates that both Croon's model of Equation III.1 and the improved Croon model of Equation III.2 offer satisfactory fitting of the experimental data, showing that the Rsd influence to the I_D mismatch is negligible across the whole range of investigated W.L values. Identical results were obtained for PMOS devices, suggesting that

the drain current mismatch and difference between NMOS and PMOS reflects the Vt and β mismatch, as well as Rsd and $|Gm/I_D|$.

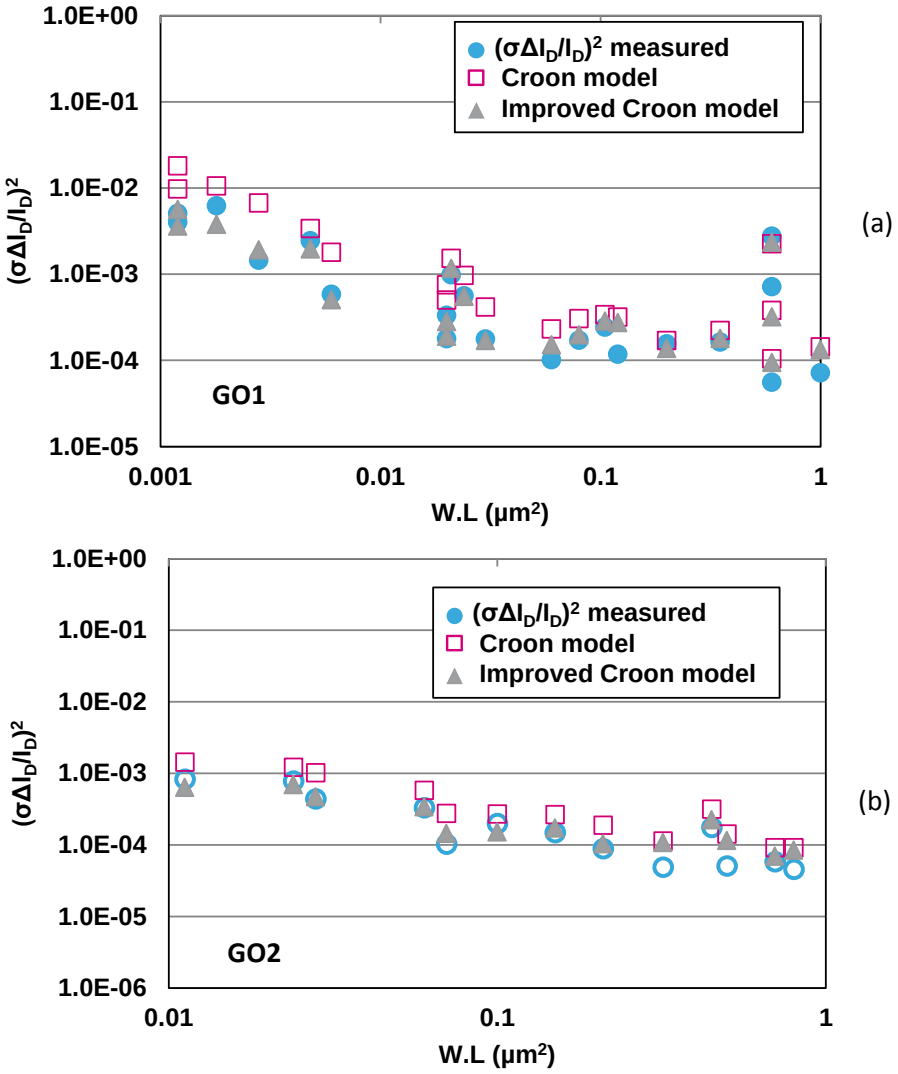


Figure VI. 5: 14nm FD SOI technology: Measured $(\sigma_{\Delta I_D/I_D})^2$, Croon's model & improved Croon Model as a function of the transistor surface W.L (µm²) for (a) GO1 and (b) GO2 NMOS devices.

VI.2.3 Comparison between 28nm and 14 nm FD SOI technologies

The results reported in the previous sections demonstrate that the Vt, β, and I_D mismatch in 14nm FD SOI technology do not scale with Tox. This section presents a comparison

between the mismatch phenomena in the 14 nm and 28 nm FD SOI technologies. Note that both devices are GO1 transistors with thin, yet different oxide thicknesses.

VI.2.3.a Threshold Voltage mismatch

The Vt values for 14nm and 28 nm FD SOI GO1 devices were first measured using the maximum slope method [Hao 95]. The results are plotted in Figure VI. 6 as a function of the gate length (L), showing that N/P MOS devices of the 14nm technology exhibit identical Vt values across the whole range of L, whereas different Vt values are observed between NMOS and PMOS devices of the 28nm technology. The plot also shows that short channel effects become evident in both 14 and 28nm FD SOI technologies at L<0.06µm.

The individual Vt mismatch parameter is thus calculated from the Vt values for 14nm and 28nm technologies and plotted in Figure VI. 7 as a function of S(µm^2). For nominal devices, very promising $iA_{\Delta Vt}$ values of 1.3mV.µm/1.4mV.µm are observed in both N/P MOS devices respectively for 14 and 28nm technologies. Furthermore, Figure VI. 7 shows that the 28 and 14 nm technologies exhibit almost identical Vt mismatch (with the exception of certain 28nm PMOS geometries), both offering very good mismatch performance. Note that an improvement in certain devices of the 14nm technology is observed ($iA_{\Delta Vt}$ = 0.9 mV.µm for W=1µm/L=0.03µm), compared to devices of the 28nm technology.

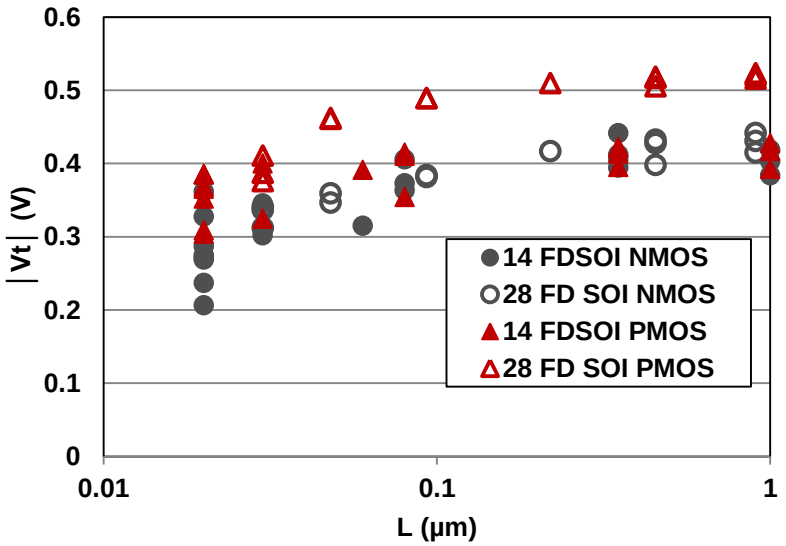


Figure VI. 6: Comparison of |Vt| (V) as a function of L (µm) between NMOS and PMOS devices of the 28nm and 14nm FD SOI technologies.

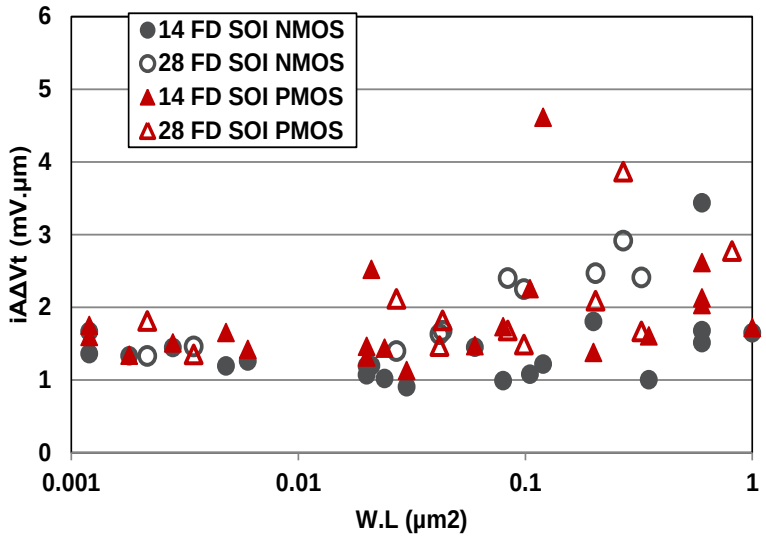


Figure VI. 7: Comparison of $iA_{\Delta Vt}$ (mV.µm) as a function of S (µm^2) between NMOS and PMOS devices of the 28nm and 14nm FD SOI technologies.

VI.2.3.b Current gain factor mismatch

The current gain factor (β) was extracted using the maximum slope method presented in [Hao 85]. The β individual constant of mismatch was then calculated using Equation I.29 for each transistor geometry. The results are plotted in Figure VI. 8, showing that the 14nm and 28 nm technologies exhibit similar β mismatch performance, both boasting excellent $iA_{\Delta\beta/\beta}$ values. The results also show that nominal NMOS devices (14 nm and 28nm technologies) exhibit better mismatch performance compared to PMOS devices. For larger dimensions, however, PMOS devices exhibit slightly better mismatch performance compared to NMOS devices.

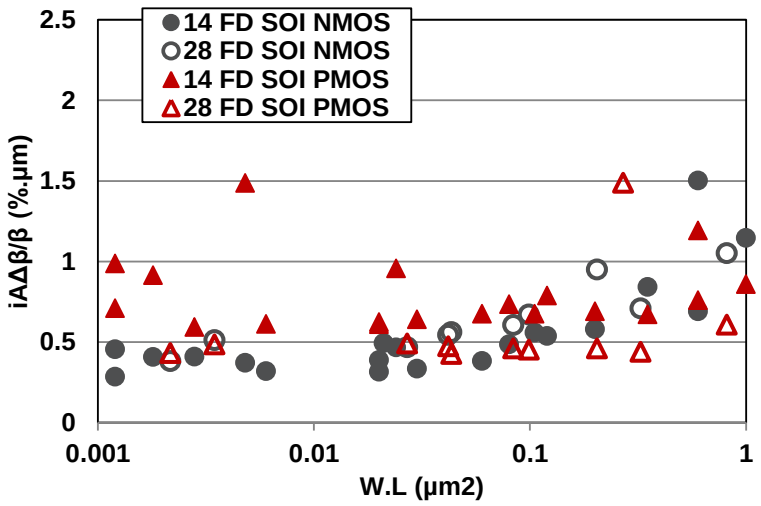


Figure VI. 8: Comparison of $iA_{\Delta\beta/\beta}$ (%.µm) as a function of S (µm^2) between NMOS and PMOS devices of the 28nm and 14nm FD SOI technologies.

VI.2.4.c Drain current mismatch

The drain current mismatch was also investigated for 14 and 28 nm N/P MOS devices. The drain current was measured in linear regime for GO1 devices. The individual constant of mismatch was then calculated using Equation I.29 and the results are plotted in Figure VI. 9. Identical mismatch behavior was observed in 14 and 28 nm technologies, with excellent mismatch performances observed in NMOS and PMOS devices. The drain current mismatch is explained by the drain current mismatch Model of Equation III.2. For 28 nm technology, this model was shown to reproduce the measured data in chapter II for NMOS and PMOS devices. As for 14 nm FDSOI technology, this model also reproduces the measured data in paragraph VI.3.3. As the Vt and β mismatch performance are similar in 14 and 28nm technologies, the drain current mismatch values are almost identical.

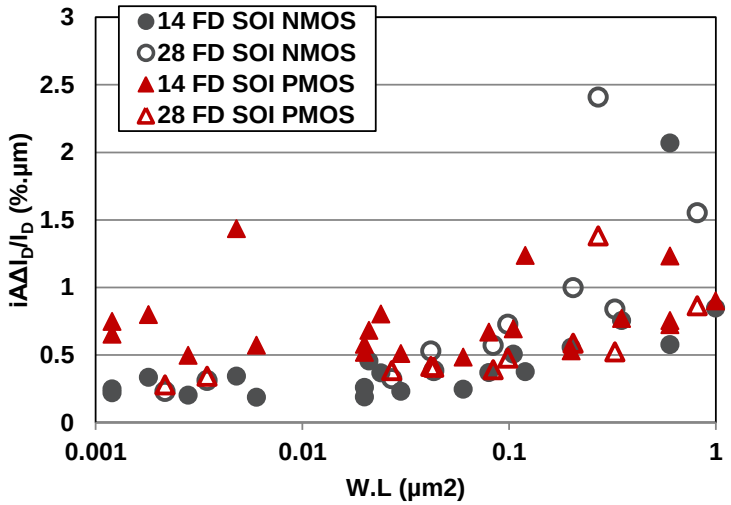


Figure VI. 9: Comparison of $iA_{\Delta I_D/I_D}$ (%.µm) as a function of the transistor surface W.L (µm^2) between NMOS and PMOS devices of the 28nm and 14nm FD SOI technologies.

VI.2.4 FD SOI technology mismatch summary and discussions

In this paragraph a plot of the electrical oxide thickness (EOT) is first presented for N/P MOS, GO1/GO2 devices of the 14 and 28 nm technologies, as shown in Figure VI. 10. This figure shows that the electrical oxide thickness of NMOS and PMOS GO1 devices of the 14 and 28 nm technologies has a variation of less than 10%. This figure also shows that the EOT for GO2 devices doubles compared to GO1 devices for both technologies and channel types.

The average values of $iA_{\Delta Vt}$, $iA_{\Delta\beta/\beta}$ and $iA_{\Delta ID/ID}$ for W.L ranging between 0.001µm^2 and 0.01µm^2 were calculated for GO1 and GO2, N/P MOS devices of the 14 and 28nm technology. The results are plotted in Figure VI. 11, Figure VI. 12 and Figure VI. 13, respectively. Figure VI. 11 shows that while the EOT doubles for GO2 devices compared to GO1 devices, similar Vt mismatch trends are observed by comparing GO1 with GO2 devices and 14 nm with 28 nm technologies.

To explain this phenomenon, Equation VI.1 is considered, which assumes as principal contributions to the Vt mismatch the gate term, represented by $\sigma_{\Phi m}^{\ 2}$, and the channel term, represented by $\frac{\sigma_{Qd}^{\ 2}}{C_{ox}^{\ 2}}$.

The conclusions of chapter V demonstrated that the Vt mismatch scales with the EOT and that the gate contribution ($\sigma_{\Phi m}^{\ 2}$ term) is negligible in advanced Bulk technologies integrating High K/ Metal gate. In FD SOI technology, however, GO1 and GO2 devices exhibit almost identical Vt mismatch values, indicating that the $\frac{\sigma_{Qd}^{\ 2}}{C_{ox}^{\ 2}}$ term is negligible and that the main contribution comes in this case from the gate stack.

$$\sigma_{\Delta V_t}^{\ 2} = \sigma_{\Phi m}^{\ 2} + \frac{\sigma_{Qd}^{\ 2}}{C_{ox}^{\ 2}} \qquad \textit{(VI. 1)}$$

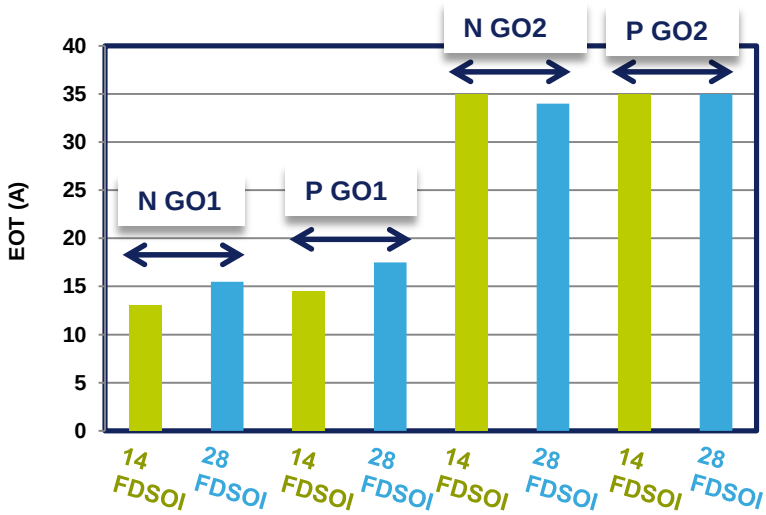


Figure VI. 10: EOT(A) values for the 28 and 14 nm technologies.

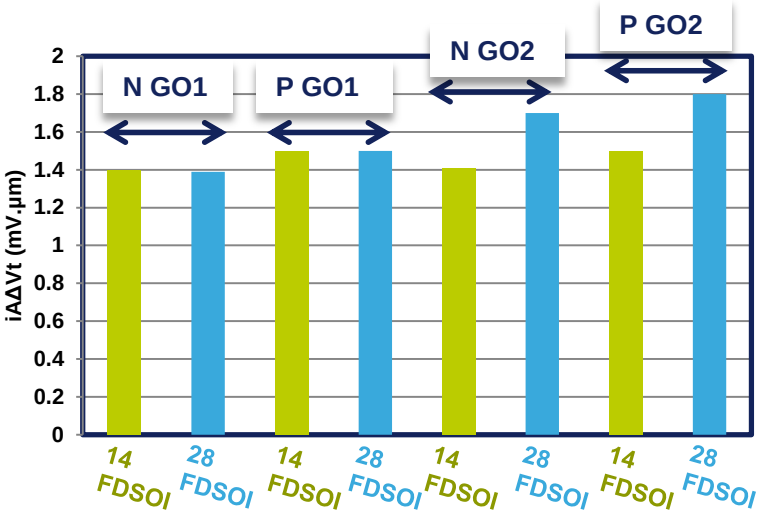


Figure VI. 11: $iA_{\Delta Vt}$ (mV.µm) mean values for the 28 and 14 nm technologies.

As for the β mismatch, the $iA_{\Delta\beta/\beta}$ values shown in Figure VI. 12 are very promising. The plot also indicates that the β mismatch, as seen in Bulk technology, does not scale with the EOT.

Finally, Figure VI. 13 shows excellent $iA_{\Delta ID/ID}$, particularly for 14 and 28 nm NMOS GO1 devices, with values of around 0.2%.µm to 0.3%.µm. Note that the I_D mismatch is mainly shaped by the Vt and β mismatch terms in Equation II.19 as was demonstrated in paragraph VI.3.3, and does not scale with the EOT.

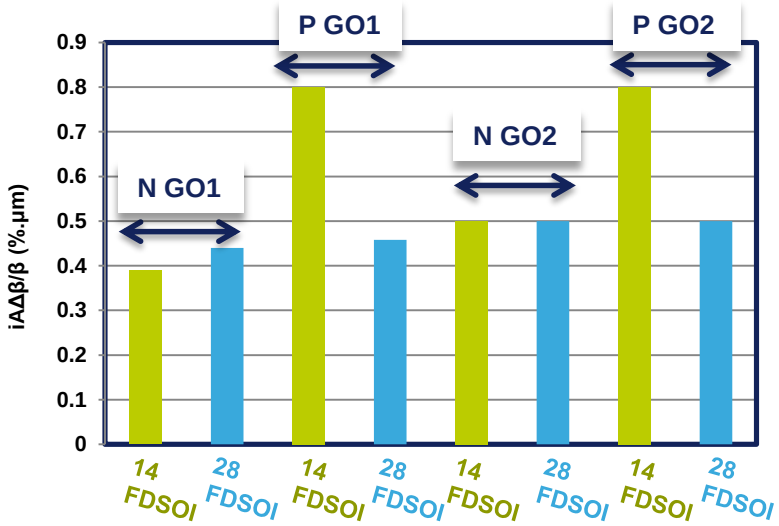


Figure VI. 12: $iA_{\Delta\beta/\beta}$ (%.µm) mean values for the 28 and 14 nm technologies.

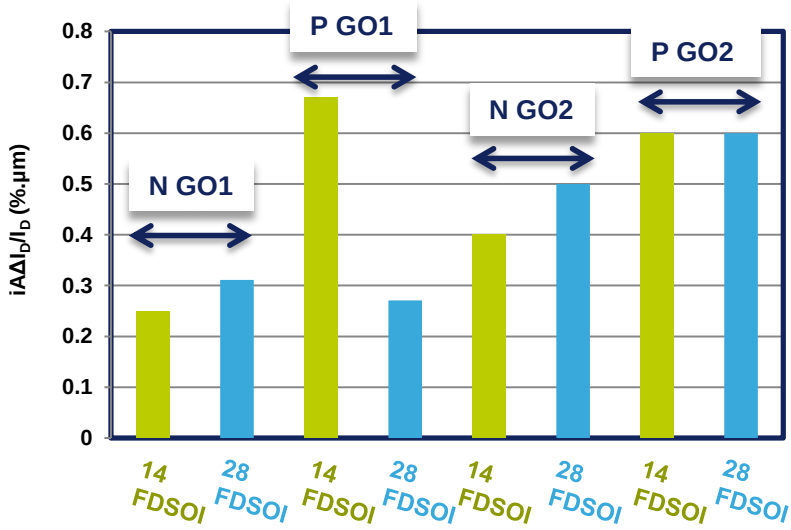


Figure VI. 13: $iA_{\Delta ID/ID}$ (%.µm) mean values for the 28 and 14 nm technologies.

VI.3 Mismatch behavior with transistor aging in response to NBTI stress

VI.3.1 Brief description of NBTI Stress

With the aim of studying the different degradation mechanisms, techniques for the acceleration of the MOS transistor's aging are used employing high voltages, accompanied in some cases by high temperatures. Such voltages are higher than the power supply voltage (V_{DD}) necessary for the optimal operation of MOS transistors. A combination of different constraints enables each degradation mechanism to be studied separately, and models of the degradation phenomena are available and constantly improved to predict the lifetime of transistors of set technology and dimensions and/or its operational behavior as a function of time such as [Arrhenius 89] [Denais 05] [Randriamihaja 12].

One of the aging tests for MOS transistors is the Negative-Bias Temperature Instability (NBTI) for PMOS devices or the Positive-Bias Temperature Instability (PBTI) for NMOS devices. The literature shows considerably higher interest in NBTI stress due to its significant impact on PMOS transistors compared to PBTI that have less impact on NMOS devices.

The NBTI stress test studies the drift of the electrical parameters of MOS transistors under application of a negative gate voltage in a high temperature environment (125°C). This is a static mechanism of degradation where the channel is maintained uniform because of the applied drain voltage equal to zero (V_{DS}=0V) as shown in Figure VI. 14.

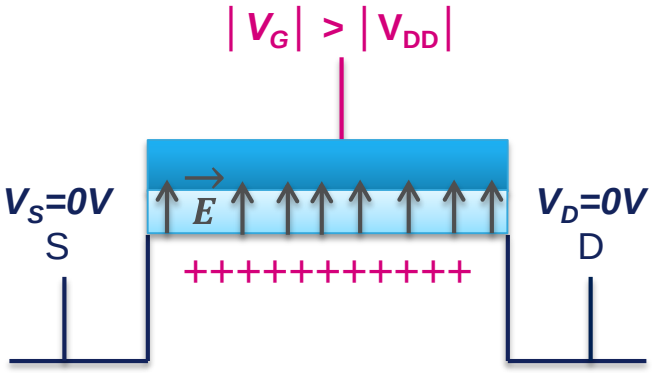


Figure VI. 14: PMOS transistor polarization in the case of NBTI stress

By applying high gate voltage to PMOS transistors, the holes in the inversion channel are confined at the Si/SiO_2 interface, interacting with the atoms and defects present in the oxide as shown in Figure VI. 15.

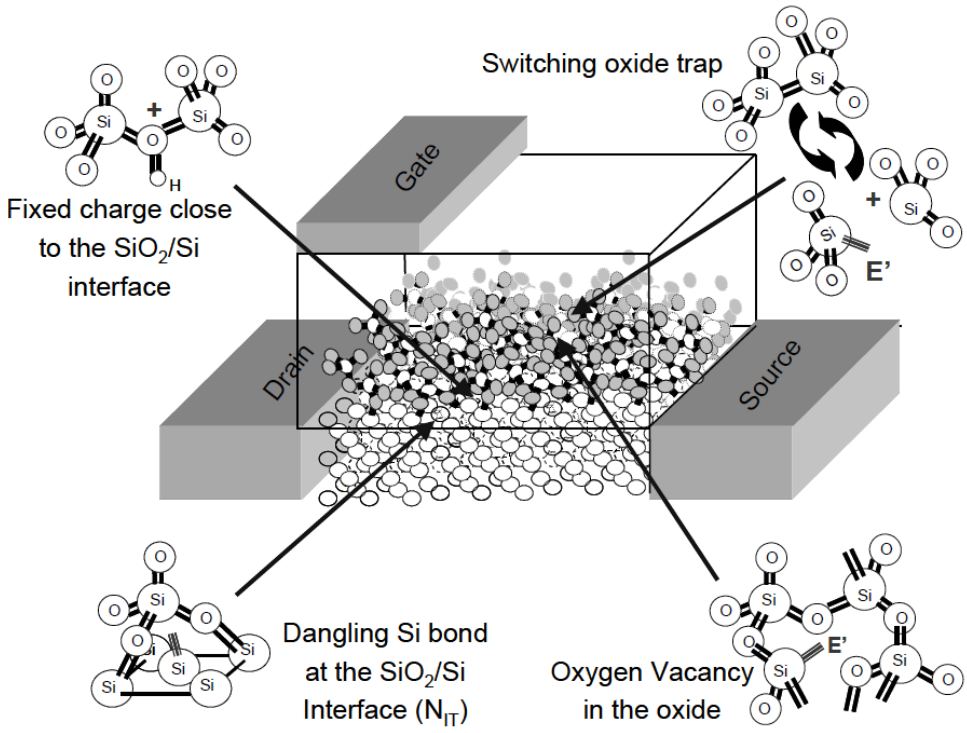


Figure VI. 15: Different interaction mechanisms between the channel holes at the Si/SiO_2 interface and the oxide atoms and defects due to NBTI stress [Denais 05].

The NBTI stress test is usually conducted by applying a high negative voltage for a given amount of time (typically between 1s and 1000s), followed by a relaxation time where the stress is stopped. Two components are observed, the recoverable component and the permanent component, as shown in Figure VI. 16.

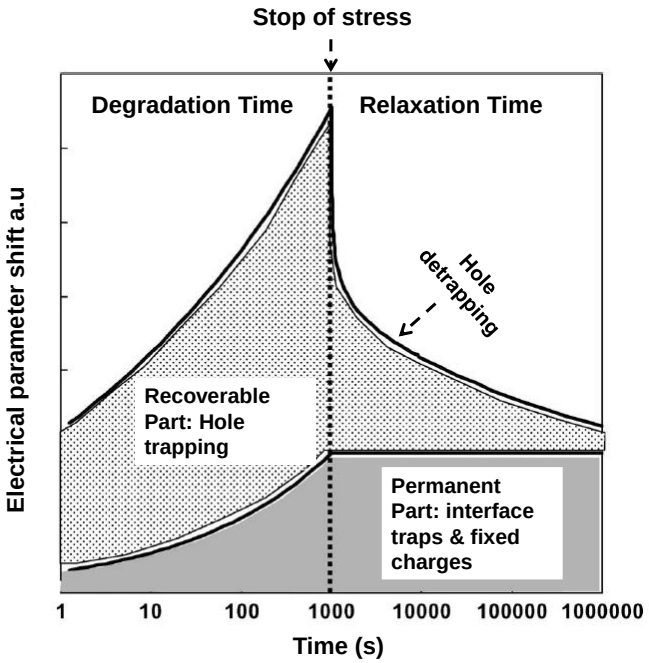


Figure VI. 16: The two NBTI stress phases and components [Huard 07]

- The recoverable part arises due to mechanisms of hole-trapping (during stress) and detrapping (after stress during the relaxation phase). The drift of the electrical parameter during the stress phase increases due to the hole trapping mechanism, only to drop to the permanent phase drift value following the detrapping phenomenon.
- The permanent part is due to the creation of interface states and fixed charges in the oxide. This component is irreversible and even after a significant relaxation time the electrical parameter under test will never revert to its previous state before stress.

The impact of interface traps and fixed charges induced by NBTI stress on the stochastic mismatch of Vt, β and I_D will be the subject of this section.

VI.3.2 Experimental details

Electrical characterization of PMOS transistors was performed on GO1 and GO2 28nm FD SOI technologies. The characteristics of the devices under test are the same detailed in section VI.2.1 and in Table VI.I. For mismatch measurements, a sample of 65 pairs of identical MOS transistors was considered.

To measure the permanent component and exclude the recoverable one, AC NBTI stress (with a duty cycle of 25%) were performed (at $|V_D| = 0V$) with gate stress voltages ranging from:

- -1.4 to -2.4V with a step of -0.1V for GO1 devices
- -3 to -4V with a step of -0.2V for GO2 devices

Additionally, for each given stress voltage value, transistor parameter measurements were conducted at the following stress time values: 0s, 10s, 40s and 100s, as shown in Figure VI. 17.

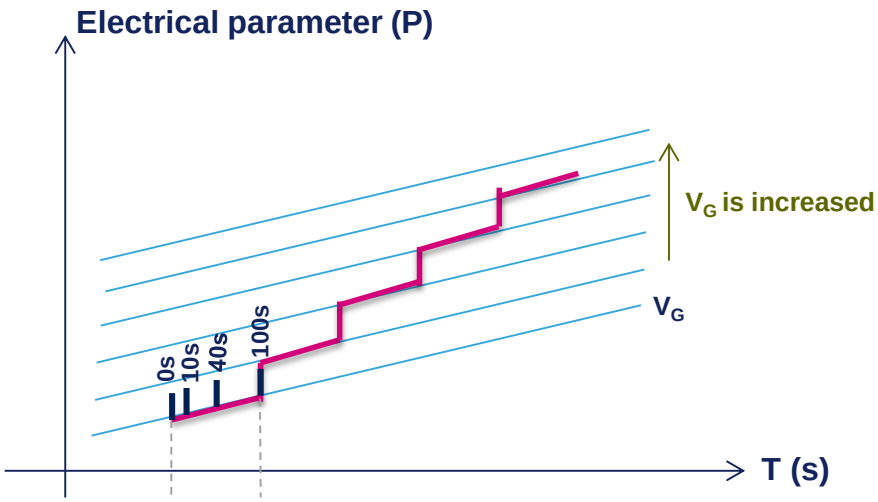


Figure VI. 17: An illustration of the electrical parameter drifts as a function of time under NBTI stress

Electrical characterization was performed:

- First on fresh transistors
- Then after each stress step

These measurements were conducted in linear regime with drain voltage $|V_D| = 0.05V$ for GO1 devices and $|V_D| = 0.1V$ for GO2 devices, and with gate voltage $|V_G| = 1V$ for GO1 devices and $|V_G| = 1.8V$ for GO2 devices.

All presented results refer to measurements performed at 125°C. In this work, the individual mismatch constant of Equation I.29 is considered. This parameter allows the evaluation of the mismatch values for each channel dimension (Section I.4.5.c).

VI.3.3 Mismatch behavior in response to NBTI stress for GO1 and GO2 28nm FD SOI devices

Tests were performed on GO1 and GO2 devices with the aim of quantifying the mismatch behavior in response to the formation of interface traps and fixed charges induced by NBTI stress. Results are then analyzed and models proposed.

VI.3.3.a Experimental results

Tests were first performed on L=0.03µm/W=0.07µm GO1 devices at 125°C. The threshold voltage (Vt) and the current gain factor (β) were extracted using the maximum slope method proposed in [Hao 85]. The drain current (I_D), was directly extracted at maximum V_G with V_D=1V. These extractions were performed on fresh transistors and at each combination of V_G and stress time.

The drifts of Vt, β and I_D are then calculated at every V_G and stress time, as shown in Equation VI.2, Equation VI.3 and Equation VI.4. The parameters' drift, calculated as absolute difference, is a direct effect of the formation of interface traps and fixed charges at the Si/SiO_2 interface and within the oxide, at each V_G value and stress time. Finally, the individual mismatch constants (Equation I.29) are calculated, for Vt, β and I_D. Results are plotted as a function of the parameters' drift respectively in Figure VI. 18.a, Figure VI. 19.b and Figure VI. 20.c.

$$\delta Vt_{Drift} = \left| Vt_{Stress} - Vt_{Fresh} \right| \qquad \textbf{(VI. 2)}$$

$$(\delta\beta / \beta)_{Drift} = 100.\left| \frac{\beta_{Stress} - \beta_{Fresh}}{\beta_{Fresh}} \right| \qquad \textbf{(VI. 3)}$$

$$(\delta I_D / I_D)_{Drift} = 100.\left| \frac{I_{D\,Stress} - I_{D\,Fresh}}{I_{D\,Fresh}} \right| \qquad \textbf{(VI. 4)}$$

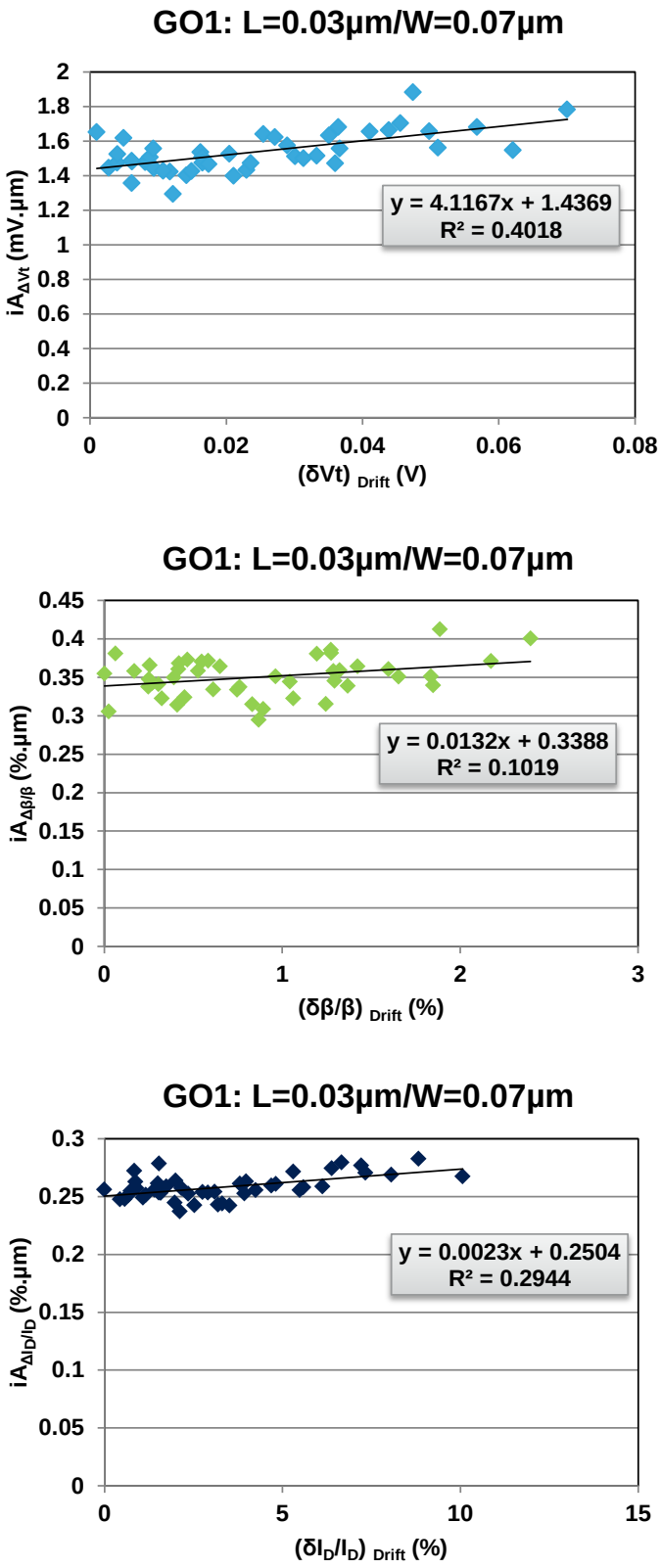


Figure VI. 18: Individual constants of mismatch (Vt (a), β (b), and I_D (c)), as a function of the drift for GO1 devices with L=0.03µm and W=0.07µm.

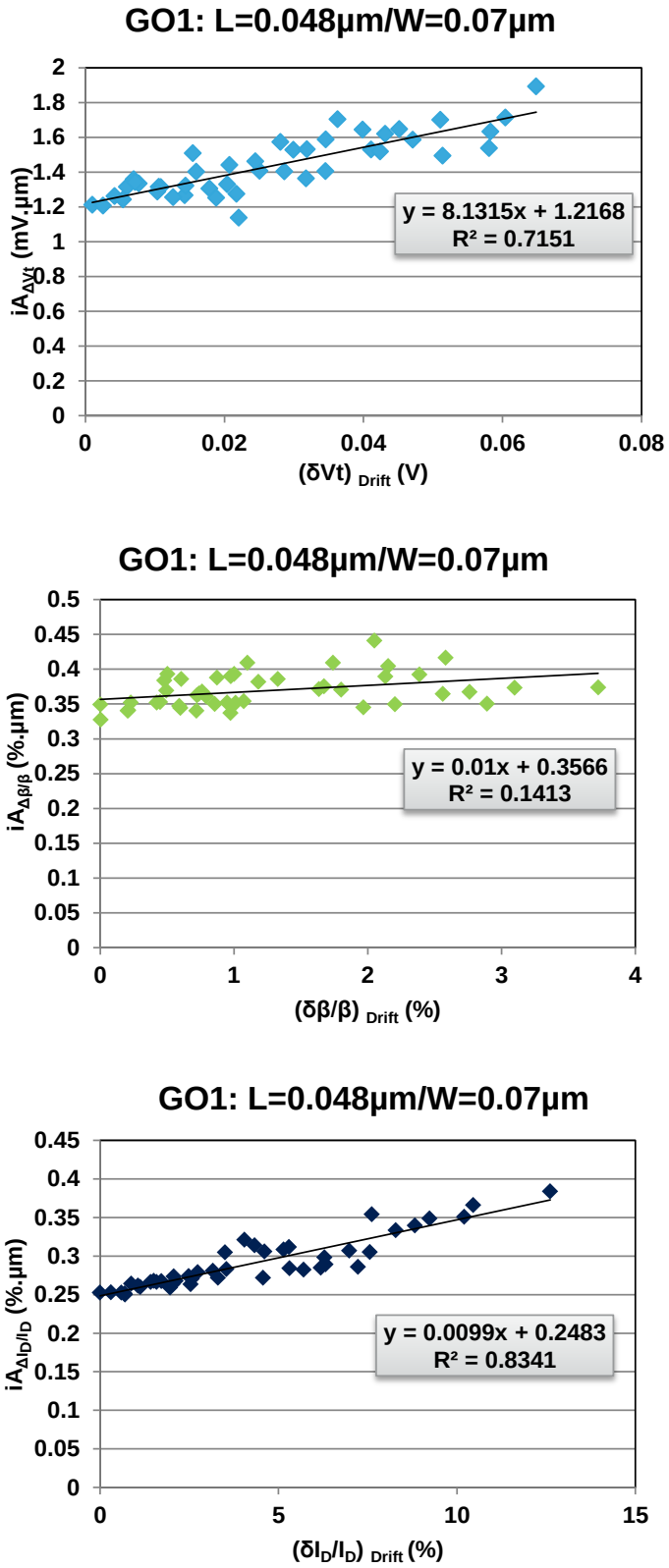


Figure VI. 19: Individual constants of mismatch (Vt (a), β (b), and I_D (c)), as a function of the drift for GO1 devices with L=0.048µm and W=0.07µm.

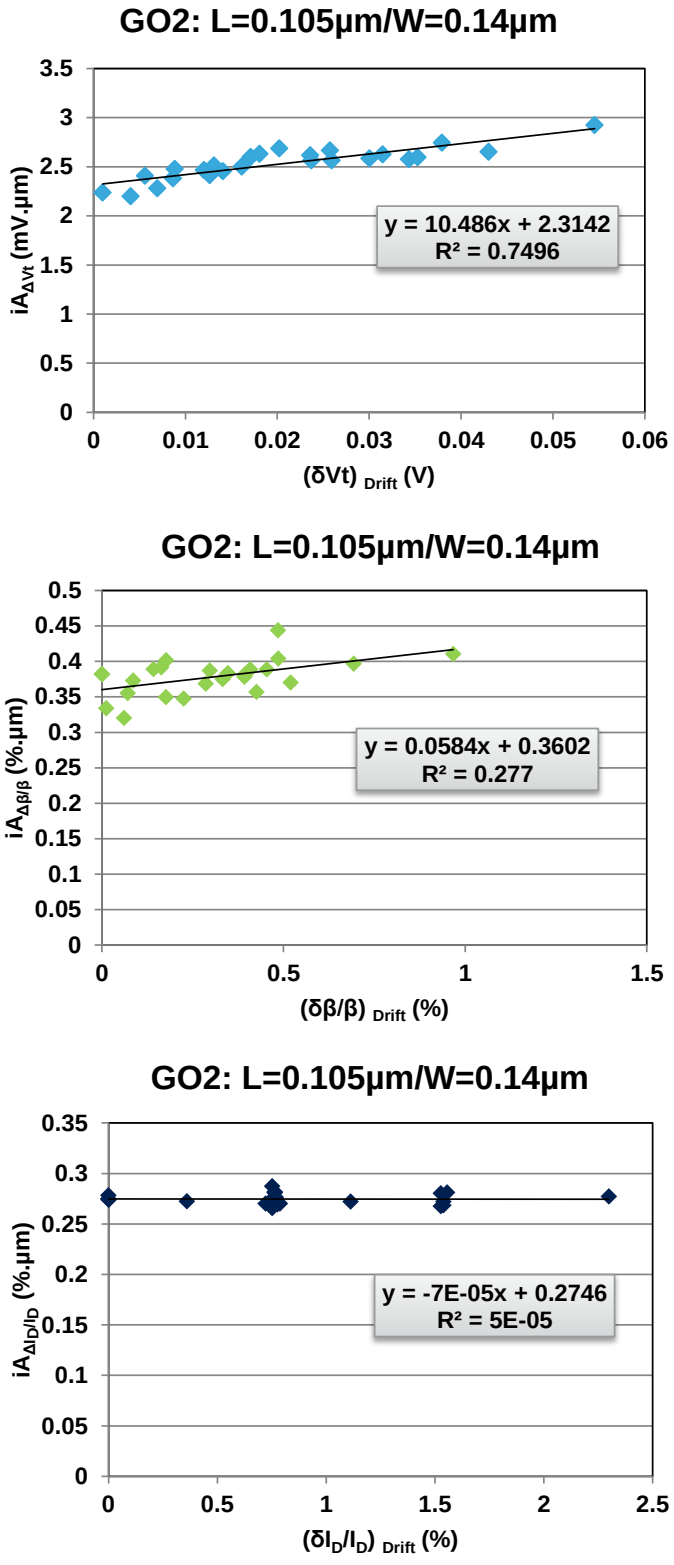


Figure VI. 20: Individual constants of mismatch (Vt (a), β (b), and I_D (c)), as a function of the drift for GO2 devices with L=0.105µm and W=0.14µm.

Figure VI. 18.a shows moderate and linear degradation of Vt mismatch as a function of $(\delta Vt)_{Drift}$ with a few correlation of 0.4 and a difference of 0.13mV.µm between the fresh and the stressed transistor at V_G= -2.4V and stress time of 100s. This is a direct effect on the $iA_{\Delta Vt}$ values of the formation of interface traps and fixed charges induced at the Si/SiO_2 interface and within the oxide at each V_G value and stress time. Moreover, very small degradation is observed in Figure VI. 18.b for the β mismatch as a function of the $(\delta\beta/\beta)_{Drift}$ with negligible correlation of 0.1 and a degradation percentage of 12.8% between the fresh and the stressed transistor at V_G= -2.4V and stress time of 100s.

For the I_D mismatch, Figure VI. 18.c does not show any significant I_D mismatch variation as a function of the $(\delta I_D/I_D)_{Drift}$ with a degradation percentage of 4.3% between the fresh and the stressed transistor at V_G= -2.4V and stress time of 100s.

The same study was performed on L=0.048/W=0.03µm GO1 devices. In this case significant Vt and I_D mismatch degradation is observed as a function of the $(\delta Vt)_{Drift}$ and $(\delta I_D/I_D)_{Drift}$, as shown in Figure VI. 19.a and Figure VI. 19.c respectively. The two plots correlations of 0.7 and 0.8 respectively between Vt mismatch and $(\delta Vt)_{Drift}$, and between I_D mismatch and $(\delta I_D/I_D)_{Drift}$. Moreover a Vt mismatch difference of 0.76mV.µm and an I_D mismatch degradation percentage of 51.9% are observed between the fresh and the stressed transistor at V_G= -2.4V and stress time of 100s. However, no significant variation of β mismatch as a function of $(\delta\beta/\beta)_{Drift}$ is observed in Figure VI. 19.b.

An identical study of Vt, β and I_D individual constants of mismatch as a function of their drift was conducted at moderate gate length and width L=0.105µm/W=0.14µm for GO2 devices (thicker oxide). Results are plotted in Figure VI. 20.a, Figure VI. 20.b and Figure VI. 20.c for the three parameters, respectively.

Figure VI. 20.a shows a linear and moderate Vt mismatch degradation as a function of $(\delta Vt)_{Drift}$ with a correlation of 0.74 and a difference of 0.68mV.µm between the fresh and the stressed transistor at V_G= -4V and stress time of 100s. Figure VI. 20.b shows very small β mismatch degradation as a function of $(\delta\beta/\beta)_{Drift}$ with negligible correlation of 0.27 and a degradation percentage of 7.5% between the fresh and the stressed transistor at V_G= -4V and stress time of 100s. Finally, no significant variations are observed for I_D as a function of its Drift, with a degradation percentage of 1.3% between the fresh and the stressed transistor at V_G= -4V and stress time of 100s.

VI.3.3.b Theoretical models and discussions

Referring to chapters II, III and V, the I_D mismatch can be explained by the mismatch of Vt and β, as well as the contributions of Gm/I_D and Rsd in Equation II.20. Analogously, the I_D mismatch variation with NBTI stress can also be explained with this equation. Note that no significant I_D variation is observed experimentally, except for L=0.048µm/W=0.07µm. The explanation of the observed behavior of Vt and β mismatch as a function of their Drift has however more complicated roots. To try to quantify the linear degradation of the Vt mismatch and the small degradation of the β mismatch in response to the effects of interface traps and fixed charges induced by the NBTI stress, models were developed for the Vt and β mismatch as a function of their Drift. This is detailed in the following paragraph.

1- Vt mismatch model as a function of the induced interface traps and fixed charges at the Si/SiO_2 interface and in the oxide:

When introducing interface traps and fixed charges at the Si/SiO_2 interface and in the oxide, the Vt Drift between fresh and stressed MOS transistors can be written as:

$$(\delta Vt)_{Drift} = \frac{qN_{st}}{C_{ox}} \qquad \textbf{(VI. 5)}$$

Where N_{st} is the concentration of the interface traps and fixed charges induced by the NBTI stress at the Si/SiO_2 interface and in the oxide

Vt stochastic mismatch of two identical MOS transistors after NBTI stress can be written i.e. using Poisson law, as:

$$\sigma^2_{\Delta Vt} = \sigma^2_{\Delta Vt0} + \frac{q^2 N_{st} WL}{(WLC_{ox})^2} \qquad \textbf{(VI. 6)}$$

Where $\sigma_{\Delta Vt0}$ is the fresh mismatch before stress, while $\frac{q^2 N_{st} WL}{(WLC_{ox})^2}$ represents the added interface traps and fixed charges at the Si/SiO_2 interface and in the oxide.

The Vt individual mismatch constant can thus be written as:

$$iA_{\Delta Vt}^2 = iA_{\Delta Vt0}^2 + \frac{q^2 N_{st}}{C_{ox}^{\ 2}} \qquad \textbf{(VI. 7)}$$

Equation VI.7 can also be written as a function of ΔVt drift as shown in Equation VI.8:

$$iA_{\Delta Vt}^2 = iA_{\Delta Vt0}^2 + \frac{q}{C_{ox}}(\delta Vt)_{Drift} \qquad \textbf{(VI. 8)}$$

N_{st} values are first chosen in a way that $(\delta Vt)_{Drift}$ in Equation VI.5 reproduces the measured data. $iA_{\Delta Vt}$ induced by the obtained N_{st} (i.e. in Equation VI.7) are then compared to measured $iA_{\Delta Vt}$ values. Results are plotted in Figure VI. 21, for L=0.03µm/W=0.07µm geometry. This figure shows that the Vt mismatch degradation model reproduces to a certain extent the measured data and can thus explain and predict the Vt mismatch behavior as a function of the Vt Drift (i.e. as a function of N_{st} values).

This model was also applied to the other geometries considered in this study as shown Table VI.2. A small underestimation of the model is observed and can be improved in future work for a better data fit. However, two important conclusions can be deduced:

1- FD SOI transistors presents moderate degradation of Vt mismatch as a function of the Vt Drift.

2- The presented model gives an estimation of the Vt mismatch as a function of N_{st} induced by NBTI stress.

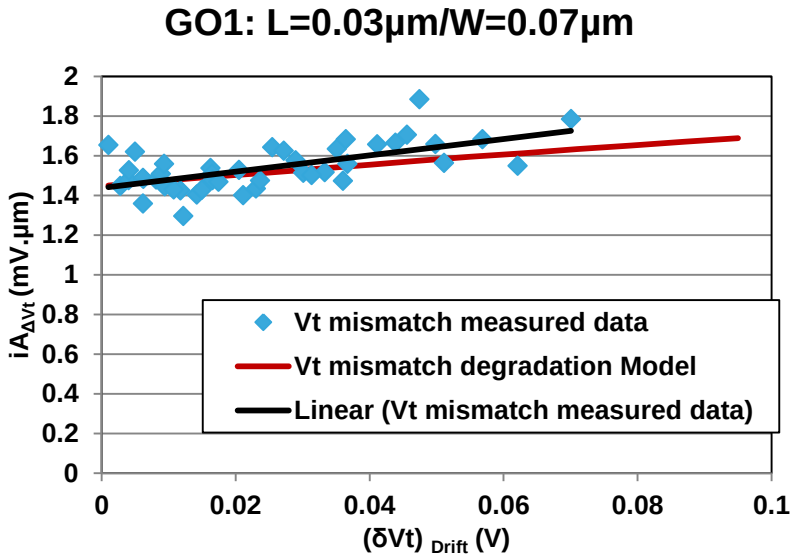


Figure VI. 21: Individual constant of Vt mismatch as a function of its Drift: comparison between measured data and theoretical degradation model for GO1 devices with L=0.03µm and W=0.07µm.

Table VI. 2: Comparison between $iA_{\Delta Vt}$ measured data and theoretical degradation model for a specific $(\delta Vt)_{Drift}$ Values

	GO1:L=0.048µm/W=0.07µm $(\delta Vt)_{Drift}$**=0.06V**	**GO2:L=0.105µm/W=0.14µm** $(\delta Vt)_{Drift}$**=0.05V**
Model: $iA_{\Delta Vt}$	1.45 mV.µm	2.52 mV.µm
Measured data: $iA_{\Delta Vt}$	1.65 mV.µm	2.78 mV.µm

2- β mismatch model as a function of the induced interface traps and fixed charges at the Si/SiO_2 interface and in the oxide:

When introducing interface traps and fixed charges at the Si/SiO_2 interface and in the oxide, the low field mobility drift ($\delta\mu_0/\mu_0$) between fresh and stressed MOS transistors, based on [Sun 80], can be written as:

$$(\frac{\delta\mu_0}{\mu_0})_{Drift} = \alpha.q.\mu_0.N_{st} \qquad \textbf{(VI. 9)}$$

Where α is the coefficient of the remote Coulomb Scattering

Using the first order Taylor approximation, and supposing that the principal contribution of β mismatch is μ_0:

$$(\frac{\delta\beta}{\beta})_{Drift} = (\frac{\delta\mu_0}{\mu_0})_{Drift} \qquad \textbf{(VI. 10)}$$

α (V.s/C^{-1}) can thus be calculated using equations VI.5, VI.9 and VI.10 in Equation VI.11:

$$(\frac{\delta\beta}{\beta})_{Drift}(\%) = \alpha.\mu_0.C_{ox}..(\delta Vt)_{Drift}.100 \qquad \textbf{(VI. 11)}$$

The β stochastic mismatch of two identical MOS transistors after NBTI stress can be written (using Poisson law) as:

$$\sigma^2{}_{\Delta\beta/\beta} = \sigma^2{}_{\Delta\beta/\beta}|_0 + \frac{\alpha^2.q^2.N_{st}.\mu_0^2.W.L}{(W.L)^2} \qquad \textbf{(VI. 12)}$$

where $\sigma^2_{\Delta\beta/\beta|0}$ is the mismatch in the fresh transistor before the application of stress, while $\frac{\alpha^2.q^2.N_{st}.\mu_0^2.W.L}{(W.L)^2}$ represents the added contribution of interface traps and fixed charges at the Si/SiO_2 interface and in the oxide.

The β individual mismatch constant can thus be written as

$$iA^2_{\Delta\beta/\beta|} = iA^2_{\Delta\beta/\beta|0} + \alpha^2.q^2.N_{st}.\mu_0^2 \qquad \textbf{(VI. 13)}$$

Equation VI.10 and Equation VI.13 were compared to the measured data for the L=0.03µm/W=0.07µm geometry. The results plotted in Figure VI. 22 show that the β mismatch model of Equation VI.13 does not predict any significant degradation as a function of $(\delta\beta/\beta)_{Drift}$, while the measured data shows a small degradation of $iA_{\Delta\beta/\beta}$ as a function of $(\delta\beta/\beta)_{Drift}$. The value assigned to α is 1.10^3, while N_{st} is varied from 1.10^{11} cm^3 to $1.2.10^{12}$ cm^3 with a step of 1.10^{11} cm^3.

Discussion about the model parameters:

- When α is increased, $iA_{\Delta\beta/\beta}$ suffers higher degradation. However, in this case the $(\delta\beta/\beta)_{Drift}$ overestimates the measured data.
- When Nst is increased, $iA_{\Delta\beta/\beta}$ also suffers higher degradation. However, $(\delta Vt)_{Drift}$ underestimates the measured data. If therefore a faithful image of the Vt mismatch as a function of $(\delta Vt)_{Drift}$ is to be maintained, the β mismatch model does not show significant degradation as a function of $(\delta\beta/\beta)_{Drift}$.

Equation VI.13 however predicts a very small degradation of $iA_{\Delta\beta/\beta}$ as a function of $(\delta\beta/\beta)_{Drift}$, that is not totally far from measured data, where the worst cases shows a degradation of 12.8%.

This model was also applied to the other geometries considered in this study and the same conclusions were observed.

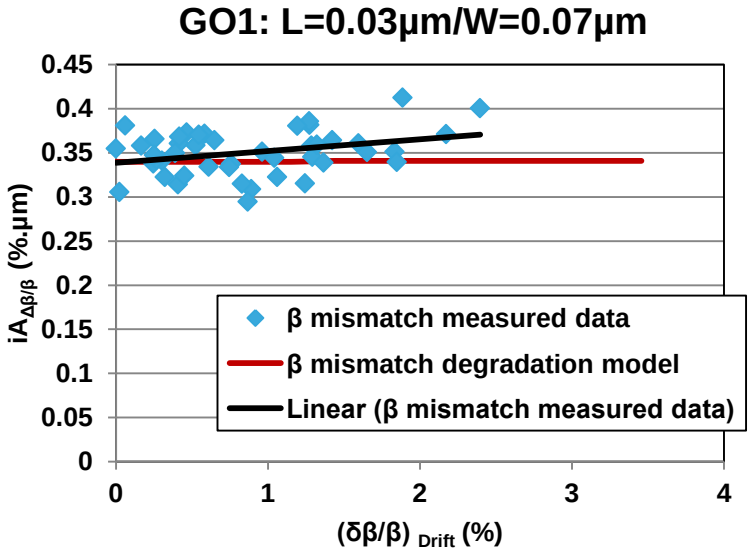


Figure VI. 22: Individual constant of β mismatch as a function of its Drift: comparison between measured data and theoretical degradation model for GO1 devices with L=0.03µm and W=0.07µm.

VI.4 Conclusions

This chapter is divided into two major sections, from which the following conclusions can be drawn.

- The first section reports an investigation of the Vt, β and I_D mismatch in 14nm FD SOI technology, along with a comparison with the 28nm FD SOI technology. The presented results indicate identical Vt, β and I_D mismatch performance in both GO1 and GO2 devices for the 14nm N/P MOS FD SOI technology. This similarity can be explained by the absence of doping in the channel, which makes the channel mismatch contribution negligible with respect to the gate contribution. This observation can be further extended by observing that, on the opposite, the contribution of the channel is dominant in the Vt mismatch for Bulk technology. As for the I_D mismatch, similar results were observed in N/P MOS GO1 and GO2 devices. This similarity can be explained by fitting the experimental data with the improved Croon model proposed in chapter 2. The excellent fit shows that the observed similarity is due to the Rsd contribution, $|Gm/I_D|$ values as well as Vt and β mismatch. With regard to the 28nm technology, the results presented in this chapter show almost identical Vt, β and I_D mismatch performance as for the 14nm technology. This also confirms that the Vt

mismatch is independent of the EOT, as opposed to what is observed in Bulk technology. The β mismatch is also independent of EOT as observed in BULK technology.

- The second section reports the investigation of Vt, β and I_D mismatch in 28nm FD SOI PMOS transistors as a function of their Drift due to the interface traps and fixed charges at the Si/SiO_2 interface and in the oxide induced by means of NBTI stress tests at 125°C. The tested devices have small or moderate areas. Results show moderate degradation of Vt mismatch as a function of the effect of the induced interface traps and fixed charges. A compact model directly dependent on the N_{st} values that can explain the observed degradation was developed and successfully applied to the measured data. This model, however, shows in some cases a slight underestimation of measured data. Future work can be considered aimed at improving this model.
  concerning β mismatch, a small degradation of 12% in worst cases and 1% in best cases was observed as a function of the $(\delta\beta/\beta)_{Drift}$. This also reflects the dependence of the induced interface traps and fixed charges at the Si/SiO_2 interface and in the oxide on the β mismatch. A compact model directly depending on the N_{st} values that can predict the β mismatch degradation was also developed. When applied to the measured data, however, this model underestimates the measured degradation. Using the same $(\delta\beta/\beta)_{Drift}$ as in the measured data, the model predicts a less pronounced $iA_{\Delta\beta/\beta}$ degradation than what experimentally measured. Nevertheless, this model can give an approximation of the measured variation, which is anyway negligible.
  Finally, for I_D mismatch, a negligible degradation as a function of the induced N_{st} was observed except for the L=0.045µm/W=0.07µm geometry. The I_D mismatch degradation results from a combination of the Vt and β mismatch, as well as Gm/I_D and Rsd contributions in Equation II.20. Thus, any variation of these parameters induces a variation in the I_D mismatch in fresh transistors. In future work this model can be applied to devices subject to NBTI stress, with the main purpose of studying the Rsd behavior in response to NBTI stress.

General Conclusions and perspectives

The work reported in this thesis provides answers relevant to the four major subject areas proposed in the general introduction.

In regards to the optimization of the measurement methodologies for mismatch phenomena, chapter II proposed:

- A method for the fast and direct extraction of Vt and β mismatch, that avoids going through the classical statistical treatment. This new extraction methodology is based on the Y function mismatch as a function of V_G. It is valid in strong inversion regime and demonstrated to be independent from the Rsd contribution. This method was successfully applied to measured data for 28nm FD SOI and Bulk technologies. However, this methodology should be used in a V_G range where θ_2 can be neglected, for example at maximum $V_G=V_{DD}$.
- A new drain current mismatch model that expands from the strategy published by Croon [Croon07] by adding a Rsd contribution term and neglecting the mutual correlation terms between parameters. This model was successfully applied to the measured data. It can give a good estimation by a comparison with the classical Croon model of the influence of R_{SD} on I_D mismatch in advanced technologies and mainly in small areas transistors. This model can provide better understanding of the I_D mismatch in advanced technologies, by identifying the main contributing factors. This can in turn enable further physical optimization

In regards to the mismatch characterization of various MOS transistor configurations for design applications, chapter III focused on the characterization of Vt, β and I_D mismatch in classical MOS, Lateral drain extended MOS (LDEMOS) and devices in cascode configuration. The study aimed at selecting the optimal architecture to guarantee good mismatch performance with the ability of sustaining high drain voltages. The reported findings showed that:

- LDEMOS, designed to sustain high drain voltages, exhibit very degraded Vt and β mismatch in linear and saturation regimes. This is due to the diffused and not well-controlled channel. In comparison, classical MOS transistor show good robustness to Vt and β mismatch, with significant improvement compared to LDEMOS devices. This is due to the better-controlled channel which eliminates a specific source of variability. However, this architecture cannot sustain as high drain voltages as LDEMOS, therefore the proposed solution is to use two classical MOS transistors connected in cascode configuration. This configuration, known to sustain as high drain voltages as the LDEMOS transistor, was demonstrated to exhibit Vt and β mismatch performance similar to individual MOS devices.

- For I_D mismatch, the three different architectures used in this study exhibit comparable performance in linear and saturation regimes. In linear regime, the new drain current mismatch model proposed in chapter II and the classical Croon model were applied to the measured data. The new model was shown to reproduce data for the three presented architectures. The results also showed that the Rsd contribution has lowest impact on cascode configuration devices and highest impact on LDEMOS devices. The similarity amongst the I_D mismatch values for the three considered architectures are mainly due to the Gm/I_D term. Double Gm/I_D values are observed in the case of individual and cascode configuration as compared to LDEMOS.

  For the saturation regime, a new drain current mismatch model was proposed based on the same approach followed for the linear regime, starting from the drain current equation. This model was successfully applied to the measured data for individual devices and devices in cascode configuration, while it overestimates the measured data for the LDEMOS architecture. In future work, further investigation of the reasons for such overestimation should be considered with the aim of improving the model.

The work presented in this part of the thesis can be adapted to fit specific applications, according to the designer's objectives. For example, considering the same drain current value for the three devices, a comparison of their corresponding area on silicon and mismatch performances can be performed. Another possible approach is to consider a set area value (same space on Silicon) for the three architectures and compare their drain current values and mismatch performances.

In regards to the analysis and modeling of advanced MOSFET technologies, 28 nm Gate-first and 20nm Gate-last BULK, 28nm FD SOI and 14nm FD SOI technologies were considered. This subject was treated in three chapters:

- In chapter IV, a complete study of Vt, β and I_D mismatch behaviors for transistors with and without germanium, and transistors with different percentages of Germanium was performed on 28nm Bulk PMOS devices integrating Highk/metal gate with and without pocket implants. The drawn conclusions can be summarized as follows.
  - No significant effect of the Ge introduction for percentages from 20% to 34% on Vt mismatch was observed for transistors without pocket implants due to:
    1. Negligible variability of valence band offset
    2. Negligible variability of SiGe layer thickness. In this case, an important conclusion was drawn: when T_{SiGe} is large enough, it does not introduce significant variability. However when T_{SiGe} becomes small (less than 5nm in our case, according to [Soussou12]) this source of variability can influence Vt mismatch.
  - Ge introduction improves the Vt mismatch for transistors with pockets. When the Ge is introduced, the pocket doping (Arsenic) tends to be diffused in the channel. The contrast between the pocket doping and the channel doping becomes lower, improving the Vt mismatch for moderate gate lengths.
  - Ge introduction improves the β mismatch for transistors with and without pocket implants. This is attributed to the reduction of Coulomb scattering events with the introduction of Ge. However, increased percentages of Ge do not induce further variations of the β mismatch.
  - Ge introduction and its increased percentage improve the drain current mismatch for transistors with and without pocket implants. This is explained by Gm/I_D parameter in Croon's model. The model however overestimates the measured data for transistors with pocket implants, suggesting that more parameters should be considered, such as the Rsd contribution.

The reported study enabled a deeper understanding of the effects of the introduction of Germanium in the PMOS channel on the mismatch of different parameters. The results showed that the introduction of Ge in the PMOS channel can

improve, in some cases, the Vt, β and I_D mismatch, as opposed to what previously reported in the literature. The study can also aid the optimization of Vt, β and I_D mismatch and provides awareness of the different effects to be taken into consideration in any future technology integrating Ge in PMOS channel, such as 14nm FD SOI.

- In Chapter V, the metal gate-last effect on Vt and β and I_D mismatch for 20nm bulk technology was investigated. Results have been compared to the 28nm metal Gate-first technology.
  - The comparison between GO1 and GO2 devices for 20nm Gate-last revealed:
    1. Better Vt and β mismatch performance for thinner gate oxide (GO1) devices due to larger gate coupling.
    2. Identical $iA_{\Delta Qd}$ values for the thinner and thicker gate oxides. This similarity suggests that Vt mismatch scales with Tox, and that the channel contribution to the Vt mismatch is more prominent than the Gate contribution. By introducing improvements in the MGG effect, the Gate-last technology enables the gate contribution to Vt mismatch to be eliminated.
    3. Similar I_D mismatch performances for devices with thinner and thicker gate oxides. This was explained by the Rsd and $\left|Gm/I_D\right|$ contributions in the new mismatch model proposed in chapter II.
  - The comparison between 20nm Gate-first and 28 nm Gate-last shows that 20nm Gate-last technology benefits from improved Vt and β mismatch performance with very promising $iA_{\Delta Vt}$ values.
  - The last important point investigated in this study was the behavior of Vt and β mismatch that was plotted as a function of Tox from 90nm ST to 20nm Gate-last IBM. These plots showed that:
    1. $iA_{\Delta Vt}$ is linear as a function of Tox with an offset greater than zero for all nodes until the 45nm Poly-gate technology. Such offset approaches zero moving from the 28nm Metal Gate technology to the 20nm Gate-last technology.
    2. $iA_{\Delta\beta/\beta}$ does not scale as a function of Tox.

This study experimentally confirmed what concluded by the simulations of Asenov *et al*. in [Asenov 00], concerning Vt mismatch improvements when using the metal gate technology. The results also showed experimentally the advantages of the Gate-last technology on the mismatch performances. The β mismatch trends as a function of Tox were also investigated for the first time. Finally, it was experimentally confirmed that the principal contribution to mismatch in Bulk 28 and 20nm technologies remains the channel doping.

- In the first section of chapter VI, the 14 nm FD SOI and 28 nm FD SOI technologies were investigated and compared.
  - Identical Vt and β and I_D mismatch performance for thinner and thicker oxides in N/P MOS 14nm FD SOI technology were observed:
    - The Vt mismatch similarity was explained by the absence of doping in the channel. This parameter does not scale with EOT, which makes the gate contribution dominant as compared to the channel contribution, contrary to what observed in the Bulk technology.
    - β mismatch similarity also showed that this parameter does not scale with Tox. This result is similar to what obtained for the Bulk technology in chapter V.
    - The new mismatch model proposed in chapter II was able to explain the similarity in the I_D mismatch. I_D mismatch is due to the contributions of Rsd, $\left|Gm/I_D\right|$ as well as Vt and β mismatch.
  - With regard to the 28nm Technology, the results showed that the Vt, β and I_D mismatch performance are almost identical to what observed in the 14nm technology. This also confirms the following.
    - Vt mismatch is independent of the EOT, as opposed to what observed in Bulk technology.
    - β mismatch is also independent of EOT, as already observed in BULK technology.

The first section of chapter VI has set the ground to a better understanding of the principal mismatch factor in advanced FD SOI technologies: the metal gate

contribution. The advantages of using FD SOI in future technologies such as 14nm was also shown, in terms of excellent mismatch performances measured in nominal devices.

Lastly, in regards to the analysis and modeling of mismatch phenomena with the transistor aging in advanced MOSFET transistors, NBTI stress conditions at 125°C were applied to 28nm FD SOI technology and the results presented in the second section of chapter VI. It was shown that:

- Vt mismatch is moderately degraded as a function of the interface traps and fixed charges at the Si/SiO_2 interface and in the oxide induced by NBTI stress. A compact model explicitly dependent on N_{st} values was developed that could explain this phenomenon. This model was successfully applied to fit the measured data.
- β mismatch is affected by a lower degradation, with a 12% degradation observed in worst cases and 1% in best cases. A compact model explicitly dependent on N_{st} values and impact on the mobility (and thus β) was developed. However, this model underestimates the measured data.
- The I_D mismatch performance are very slightly affected by the NBTI stress, except for the L=0.045µm/W=0.07µm geometry. For fresh transistors, this mismatch behavior was shown to be a combined result of Vt and β mismatch as well as Gm/I_D and Rsd contributions in Equation II.20. However, in future work the model of Equation II.20 can be applied to stressed devices with the aim of analyzing the Rsd behavior and impact on I_D mismatch in response to NBTI stress.

This last part of the thesis showed that the FD SOI technology exhibits moderate variations in Vt mismatch and very small variations in β mismatch. Models were also proposed that can be used to estimate the Vt and β mismatch degradations as a function of the Drift of such parameters. The models can be applied, adapted or improved for other technologies such as 14 nm FD SOI or 28nm Bulk technologies.

Author publications

International Conferences:

- "Mismatch trends in 20nm Gate-last bulk CMOS technology" **Lama RAHHAL**, Aurelie BAJOLET, Jean-Philippe MANCEAU, Julien ROSA, Stephane RICQ, Sebastien LASSERE, Gerard GHIBAUDO, ULTIMATE INTEGRATION ON SILICON (ULIS), pp.133-136 , Stockholm, Sweden April 2014

- "Cascode configuration as a substitute to LDE MOSFET for improved electrical mismatch performance", **Lama RAHHAL**, Guillaume BERTRAND, Aurelie BAJOLET, Julien ROSA, Gerard GHIBAUDO, 2014 IEEE International Conference on Microelectronic Test Structures (ICMTS), pp. Udine, Italy, March 2014

- "BTI variability Fundamental understandings and Impact on digital logic by the use of extensive dataset" D. Angot, V. Huard, **L. Rahhal**, A. Cros, X. Federspiel, A. Bajolet, Y. Carminati, M. Saliva, E. Pion, F. Cacho, A. Bravaix, 2013 IEEE International Electron Devices Meeting (IEDM), pp. 15.4.1-15.4.4, 2013

- "New methodology for drain current local variability characterization using Y function method", **L. RAHHAL**, A. BAJOLET, C.DIOUF, A.CROS, J.ROSA, N.PLANES, G.GHIBAUDO, 2013 IEEE International Conference on Microelectronic Test Structures (ICMTS), pp 99 -103, Osaka, Japan, March 2013

Journals:

- "A comparative mismatch study of the 20nm Gate-last and 28nm Gate-first bulk CMOS technologies" **Lama RAHHAL**, Aurelie BAJOLET, Jean-Philippe

MANCEAU, Julien ROSA, Stephane RICQ, Sebastien LASSERE, Gerard GHIBAUDO, Solid State Electronics V. pp., 2014

- "Impact of Ge proportion on advanced SiGe bulk P-MOSFET matching performances", **Lama Rahhal**, Aurélie Bajolet, Antoine Cros, Cheikh Diouf, Flore Kergomard, Julien Rosa, Gregory Bidal, Raul-Andres Bianchi, Gérard Ghibaudo, Solid State Electronics V.85 pp 15-22, 2013

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Appendix A

Croon's Model [Croon 07], expressed by Equation A.1, and the Improved Croon Model integrating the correlation between parameters in Equation A.2 are considered.

A comparison of Equations A.1 and A.2 with and without the correlation term is provided. The results relative to 20nm Gate-Last GO2 transistors as per Chapter V/ Section V.3.3 are plotted in Figure A.1. The drain current was measured at maximum V_G of 1.8V. The graph clearly shows that at maximum V_G, the correlation term is negligible in both Croon's model and in the improved Croon model. Identical results are obtained for GO1 devices and for all the devices characterized in this thesis.

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{G_m}{I_D}\right)^2 .\sigma^2_{\Delta Vt} + \sigma^2_{\Delta\beta/\beta} - 2\frac{G_m}{I_D}\sigma_{\Delta V_T}.\sigma_{\Delta\beta/\beta}.\rho(\Delta Vt, \Delta\beta/\beta) \qquad \textit{(A. 1)}$$

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{G_m}{I_D}\right)^2 .\sigma^2_{\Delta Vt} + (1 - G_d.R_{sd})^2 .\sigma^2_{\Delta\beta/\beta} - \ldots$$
$$-2\frac{Gm}{I_D}.(1 - G_d R_{sd}).\sigma_{\Delta V_T}.\sigma_{\Delta\beta/\beta}.\rho(\Delta Vt, \Delta\beta/\beta) \qquad \textit{(A. 2)}$$

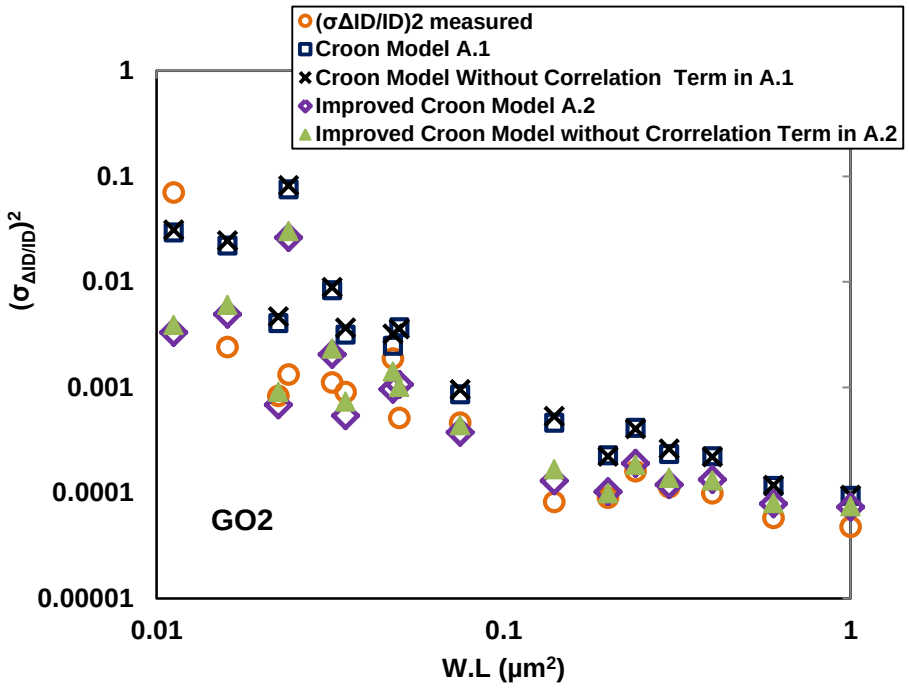

Figure A.1: Comparison between Croon's Model and Improved Croon Mode, with and without the correlation term for GO2 20nm Gate-Last devices, as per Chapter V/ Section V.3.3.

Appendix B

Thesis Abstract in French / Résumé de thèse en Français

B.I Introduction Générale

Comme son nom le suggère, le domaine de la microélectronique s'intéresse à l'études et à la fabrication des composants électroniques à l'échelle micro et nanométrique, connectés ensemble sur un même substrat formant ainsi des circuits intégrés (CI). Leurs rôle est d'implémenter une ou plusieurs fonctions électroniques plus ou moins complexes sur une même puce. Les CI sont utilisés dans des domaines très variés, comme les smart phones, la télévision, les cartes crédits, les ordinateurs, les consoles de jeux vidéo, les dispositifs pour automobiles, les applications militaires et aéronautiques. Tout progrès, dans les perspectives d'améliorer ces systèmes, débute par une amélioration du domaine de la microélectronique. L'amélioration des performances des CI consiste principalement en l'augmentation de la vitesse et la densité d'intégration, et en la réduction de la consommation d'énergie et des coûts de production.

Les éléments de base des circuits intégrés sont : les transistors, les diodes, les résistances, les condensateurs et les inductances. En 1965, Gordon Moore dans [Moore 65] prédit que le nombre des transistors présents dans un circuit d'une taille donnée sera doublé chaque année, permettant une augmentation exponentielle de ses performances. En 1975, Moore a révisé sa prédiction dans [Moore75], en affirmant que le nombre de transistors dans les processeurs va doubler tous les deux ans. Cette prédiction est connue sous 'la loi de scaling'. Le MOS de taille miniaturisée atteint un courant de saturation assez élevé, qui se traduit par une croissance de la vitesse de l'opération des produits. Le défi sera alors de préserver un courant de fuite suffisamment bas afin de limiter leurs consommations, en particulier s'ils sont alimentés par des batteries.

Un autre défi imposé par la 'loi de scaling' est la maitrise de la variabilité locale du transistor MOS. Cette variabilité locale est une conséquence des fluctuations aléatoires du processus de fabrication. Ces fluctuations causent des comportements électriques différents entre deux transistors appariés. Ainsi, il est important, pour l'industrie de la microélectronique

de comprendre les causes physiques d'une telle variabilité électrique, de les quantifier et de proposer des solutions pour les réduire.

B.II Motivations et objectifs de cette thèse

Afin de réaliser correctement leur fonction, certain blocs analogiques ou numériques comme les miroirs de courant ou les Static Random Access Memory (SRAM)) nécessitent des paires de transistors MOS électriquement identiques. Cependant, les dispositifs sur silicium, même appariés, subissent des variations locales aléatoires (comme le nombre de dopants), ce qui fait varier leurs performances électriques. Ce phénomène est connu sous le nom désappariement ou 'mismatch' en anglais.

Dans les années 1980, Pelgrom dans [Pelgrom89] a posé les fondements des études de désappariement en montrant que l'écart-type de la différence d'un paramètre P (notée ΔP) mesuré sur une paire de transistor MOS est directement lié à la surface S du transistor par la loi suivante :

$$\sigma_{\Delta P} = \frac{A_P}{\sqrt{S}} \qquad \textbf{(B. 1)}$$

La miniaturisation des transistors, suivant la loi de scaling, ainsi que la complexification de leurs procédés de fabrication ont induit des déviations de la loi de Pelgrom. Ainsi A_P n'est plus une constante. On définit alors une constante individuelle de désappariement $iA_{\Delta P}$ qui sera calculée pour chaque géométrie du transistor MOS avec :

$$iA_{\Delta P} = \sigma_{\Delta P}.\sqrt{S} \qquad \textbf{(B. 2)}$$

Dans ce cadre, les objectifs de ce travail de thèse sont :

- D'optimiser les méthodologies de mesures des phénomènes de désappariement ;
- De caractériser différentes configurations de transistors MOS afin de proposer l'architecture optimale en fonction de l'application visée;

- D'analyser et modéliser les phénomènes de désappariement observés dans les technologies avancées, notamment sur Silicium sur isolant complètement déserté (FD SOI) et sur substrat massif (Bulk).

- D'analyser et modéliser les phénomènes de désappariement en fonction du vieillissement des transistors MOS pour des technologies avancées.

B.III Principaux résultats et conclusions générales

Le chapitre I de la thèse est un chapitre introductif. Il met en relief les principaux concepts théoriques du transistor MOS classique et ces différentes méthodologies de mesures. Il introduits les différents types de variabilité électrique, notamment la variabilité globale et la variabilité locale. La variabilité locale ou désappariement est ainsi détaillée en la séparant en désappariement systématique et désappariement stochastique. Les causes de désappariement systématique et stochastique, ces méthodes d'extraction, ces effets ainsi que ces systèmes de mesures et structures de tests sont ensuite abordés. Un état de l'art des travaux précédents dans l'étude du désappariement des transistors MOS de technologie Bulk est ainsi proposé. Finalement les améliorations des performances électriques du désappariement des transistors MOS avec l'introduction de la technologie SOI sont discutées en détails en fournissant un état de l'art des travaux précédents de cette technologie.

Le chapitre II porte sur l'optimisation des méthodologies de mesures des phénomènes de désappariement. En particulier il propose :

1- Une nouvelle méthode d'extraction de désappariement de Vt et de β à partir du désappariement de la fonction Y [Ghibaudo 88]. Cette méthode est basée sur l'équation B.3. Elle est valide en régime de forte inversion et permet une extraction directe et rapide de $\sigma_{\Delta Vt}$ et $\sigma_{\Delta\beta/\beta}$ en traçant $\sigma^2_{\Delta Y/Y}.(V_G - Vt)^2$ en fonction de $(V_G - Vt)^2$. Cette méthode permet également de s'affranchir de la contribution de la résistance série source/drain (Rsd) grâce à l'utilisation de la fonction Y.

$$\sigma^2_{\Delta Y/Y} = \frac{\sigma^2_{\Delta Vt}}{(V_G - Vt)^2} + \frac{1}{4}\sigma^2_{\Delta\beta/\beta} \qquad \textbf{(B. 3)}$$

L'équation B.3 a été appliquée avec succès sur des mesures issues des technologies 28nm FD SOI et Bulk comme le montrent les Figures B.1 et B.2 respectivement. Les valeurs de $\sigma_{\Delta Vt}$ et $\sigma_{\Delta\beta/\beta}$ obtenues par cette méthode ont été comparées à la méthode classique d'extraction de $\sigma_{\Delta Vt}$ et $\sigma_{\Delta\beta/\beta}$ dans le tableau B.1 pour la technologie FDSOI. En effet, la méthode classique consiste à extraire Vt et β en utilisant la fonction Y pour N paires de transistors MOS, puis à calculer ΔVt et Δβ/β pour les N paires. Un filtre récursif est alors appliqué afin d'éliminer les valeurs erronées à l'extérieur de la moyenne ±3σ. Une fois ce traitement effectué, les écarts types $\sigma_{\Delta Vt}$ et $\sigma_{\Delta\beta/\beta}$ sont calculés.

Les résultats du Tableau B.1 montrent une similarité entre la nouvelle méthode d'extraction et la méthode classique (détaillée dans la thèse). Notons que la même comparaison a été faite avec succès sur la technologie Bulk.

Une réflexion sur les limitations de cette nouvelle méthode a également été menée. En effet cette méthode ne doit être utilisée que pour des valeurs de V_G modérées, dans une zone où le paramètre d'atténuation de la mobilité (θ_2) peut être négligeable.

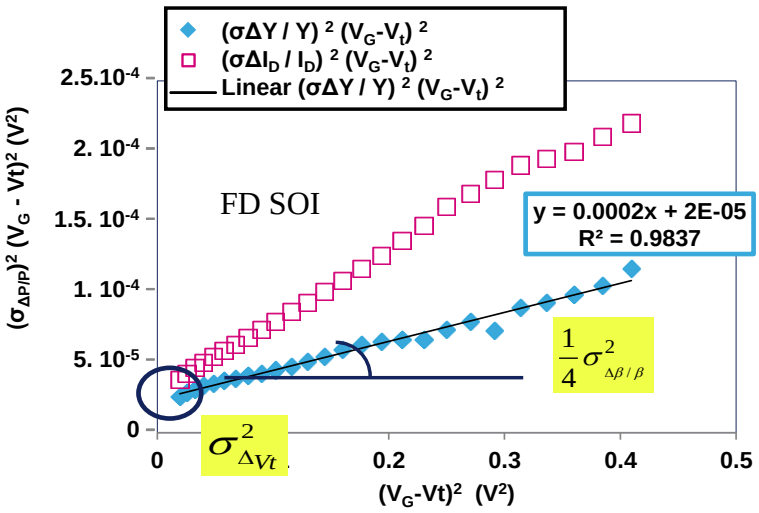

Figure B.1 : V_G>V_t (V_G varie de 0.6 à 1V avec Vt=0.36V), la fonction Y et le désappariement de courant de drain sont multipliés par $(V_G\text{-}Vt)^2$ et tracés en fonction de $(V_G\text{-}Vt)^2$ (pour des transistors FD SOI avec W=1µm/L=0.1µm et V_D =50mV)

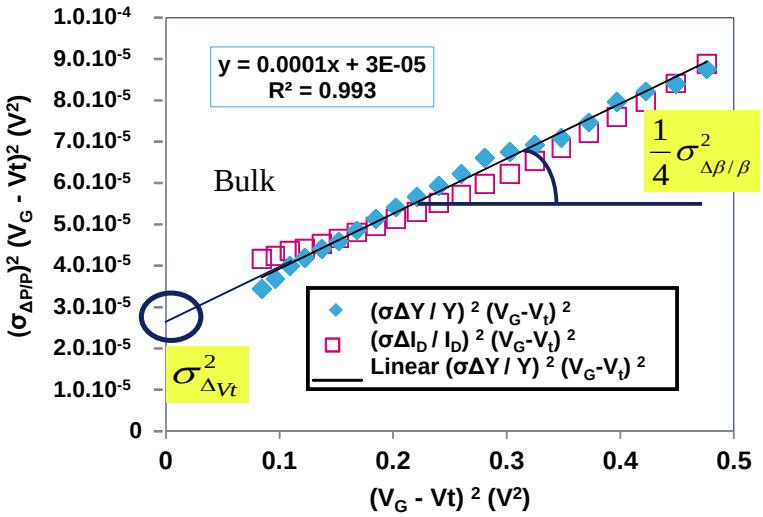

Figure B.2 : V_G>V_t (V_G varie de 0.6 à 1V avec Vt=0.31V), la fonction Y et le désappariement de courant de drain sont multipliés par $(V_G\text{-}Vt)^2$ et tracés en fonction de $(V_G\text{-}Vt)^2$ (pour des transistors BULK avec W=10µm/L=0.03µm et V_D =50mV)

Tableau B.1: Comparaison entre les désappariements de Vt et de β extraits par la méthode classique et la nouvelle méthode pour des transistors FD SOI de W=1µm/L=0.1µm

$(\sigma Paramètre)^2$	**$(\sigma_{\Delta Vt})^2$**	**$(\sigma_{\Delta\beta/\beta})^2$**
Valeurs de désappariement extraites par la méthode classique	$3.10^{-5}\,V^2$	9.10^{-4}
Valeurs de désappariement extraites par la nouvelle méthode d'extraction	$2.10^{-5}\,V^2$	8.10^{-4}

2- Un nouveau modèle de désappariement de courant de drain : Ce modèle dérive de la stratégie publiée par Croon dans [Croon 02]. En effet, à partir du modèle de Croon (Equation B.4), nous avons ajouté la contribution de Rsd et négligé la corrélation mutuelle entre les paramètres. Ce nouveau modèle (Equation B.5), est valide en régime de forte inversion et en régime linéaire.

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{Gm}{I_D}\right)^2.\sigma^2_{\Delta Vt} + \sigma^2_{\Delta\beta/\beta} - 2\frac{Gm}{I_D}\sigma_{\Delta V_T}.\sigma_{\Delta\beta/\beta}.\rho(\Delta Vt, \Delta\beta/\beta) \qquad \textbf{(B. 4)}$$

$$\sigma^2_{\Delta I_D/I_D} = \left(\frac{Gm}{I_D}\right)^2.\sigma^2_{\Delta Vt} + (1 - Gd.Rsd)^2.\sigma^2_{\Delta\beta/\beta} \qquad \textbf{(B. 5)}$$

Le nouveau modèle de désappariement de I_D dans l'équation B.5 ainsi que le modèle publié par Croon dans Equation B.4 ont été appliqués aux valeurs mesurées sur les technologies 28nm FD SOI et Bulk. Les résultats sont présentés dans les Figures B.3 et B.4 respectivement. Ces dernières montrent que le modèle de Croon ne reproduit pas les mesures pour les technologies avancées. Tandis que le nouveau modèle proposé dans cette étude dans l'équation B.5 arrive à reproduire les mesures en ajoutant la contribution de Rsd au modèle de Croon.

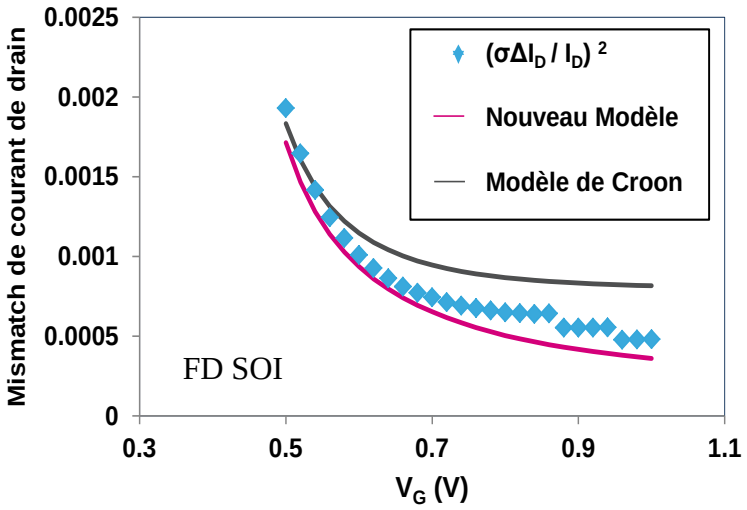

Figure B.3 : V_G>V_t (V_G varie de 0.6 à 1V avec Vt=0.36V), Comparaison entre le nouveau modèle de désappariement de courant de drain, le modèle proposé par Croon et les valeurs mesurées en fonction de V_G (transistors FD SOI avec W=1µm/L=0.1µm et V_D =50mV, Rsd=220Ω)

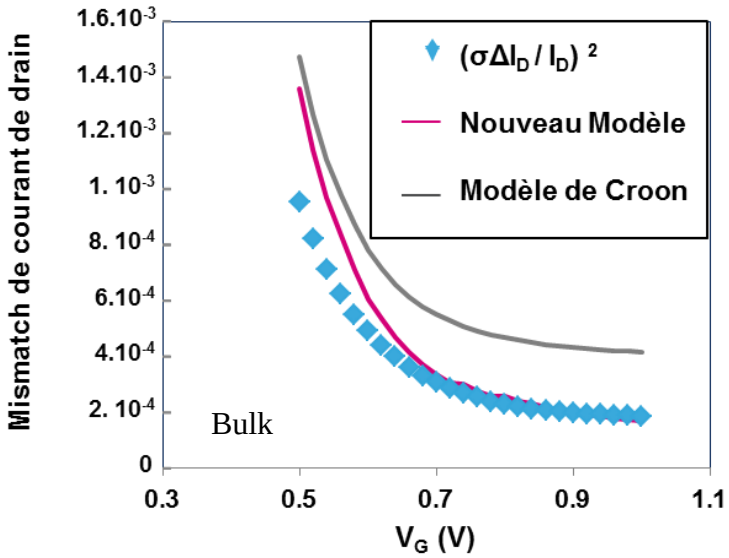

Figure B.4: V_G>Vt (V_G varie de 0.5 à 1V avec Vt=0.31V), Comparaison entre le nouveau modèle de désappariement de courant de drain, le modèle proposé par Croon et les valeurs mesurés en fonction de V_G (transistors Bulk avec W=1µm/L=0.03µm et V_D =50mV, Rsd=23Ω)

Ce nouveau modèle donne une estimation de l'influence de Rsd sur le désappariement de I_D en le comparant avec le modèle de Croon classique, notamment pour les technologies avancées et les petites géométries. L'intérêt de ce modèle est de fournir une meilleure compréhension du désappariement de I_D, grâce à une identification de ces principaux contributeurs.

Le chapitre III rentre dans le thème de caractérisation des différentes configurations de transistor MOS dans le but de proposer l'architecture optimale en fonction de l'application visée. Il présente une caractérisation du désappariement de Vt, β et I_D du transistor MOS classique illustré dans la Figure B.5, du Lateral drain extended MOS (LDEMOS) illustré dans la Figure B.6 et de la configuration cascode illustrée dans la Figure B.7. L'objectif est de proposer l'architecture optimale qui regroupe des bonnes performances de désappariement ainsi que la possibilité de maintenir des hautes tensions de drain.

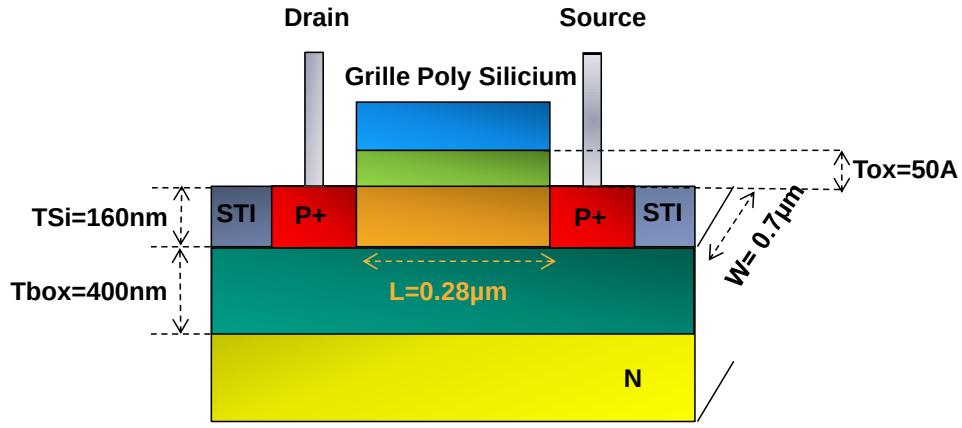

Figure B.5 : Transistor PMOS partiellement dépleté, contient un oxyde épais (Tox=5nm) avec la géométrie L=0.28µm and W=0.7µm

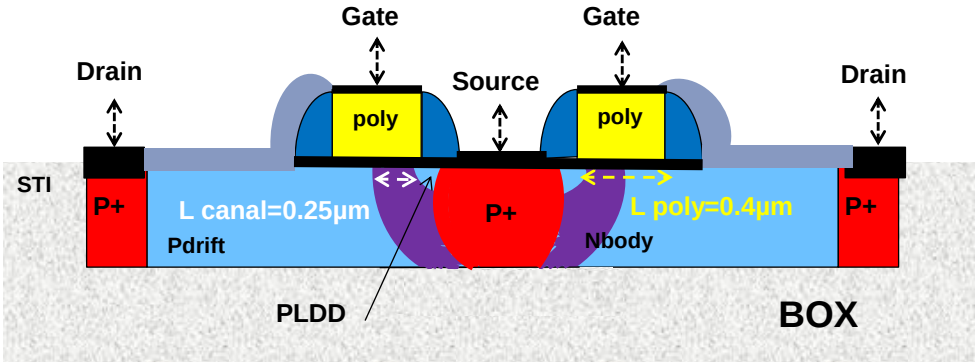

Figure B.6 : PLDE MOS, le dispositif est fabriqué sur SOI, avec une grille poly-silicium de longueur L=0.4µm, un oxyde de grille de 5nm d'épaisseur, et un Box d'épaisseur (tBox) de 400nm, l'épaisseur du SOI (tSi) est de 160nm et une épaisseur de canal estimée de 0.25µm

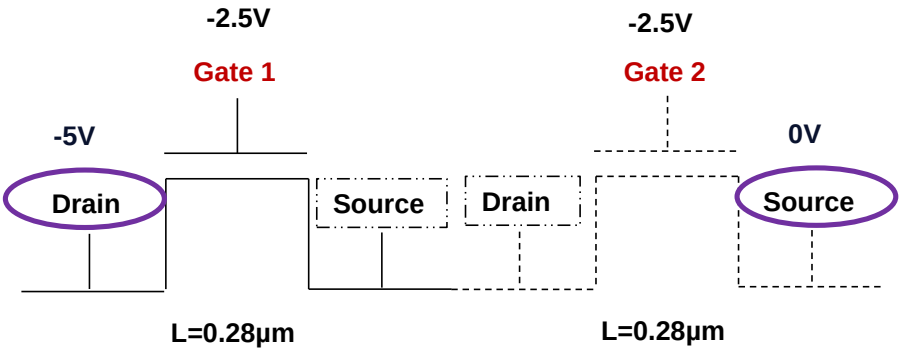

Figure B.7 : Deux transistors MOS classique connectés en configuration cascode avec L1=L2=0.28µm and W=0.7µm

Les résultats présentés dans ce chapitre ont montré que :

1- Le transistor LDEMOS, connu dans la littérature pour sa capacité à maintenir de hautes tensions de drain, a des valeurs de désappariement de Vt et de β très dégradées en régimes linéaire et saturé. Cela est dû à son canal diffusé et mal contrôlé comme le montre la figure B.6. En comparaison, le transistor MOS classique présente de très bonnes valeurs de désappariement de Vt et de β grâce à son bon contrôle dimensionnel du canal, supprimant ainsi cette source de variabilité. Cependant ce dernier n'a pas la capacité de maintenir des hautes tensions de drain. La solution proposée dans cette thèse est d'utiliser la configuration cascode de la figure B.7. Cette configuration connue pour sa capacité à maintenir autant de tension de drain que le LDEMOS, présente des valeurs de désappariement de Vt et de β proches du transistor MOS classique. Un exemple de la comparaison du désappariement de Vt des trois architectures est représenté dans la figure B.8 en régime linéaire.

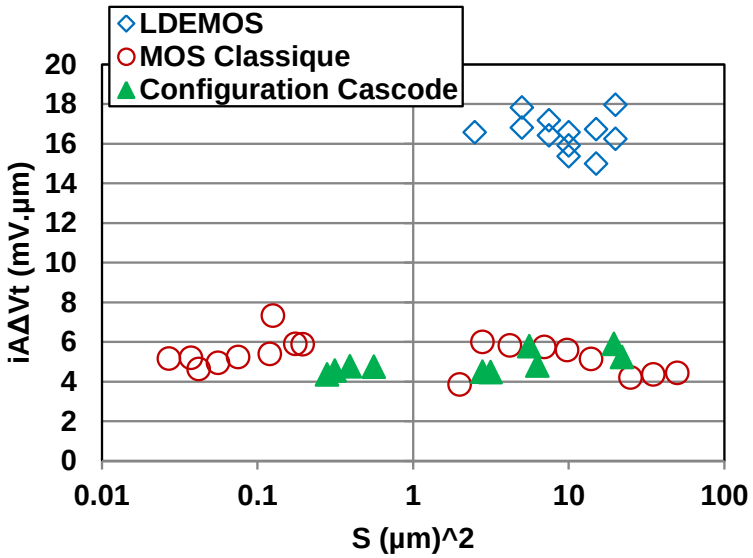

Figure B.8 : Comparaison du désappariement de Vt en fonction de la surface des transistors entre le MOSFET classique, le PLDE MOS et la configuration cascode (en régime linéaire)

2- Concernant le désappariement de I_D, les résultats ont montré des valeurs comparables entre les trois architectures du transistor MOS considérées en régime linéaire dans la Figure B.9 ainsi qu'en régime de saturation.

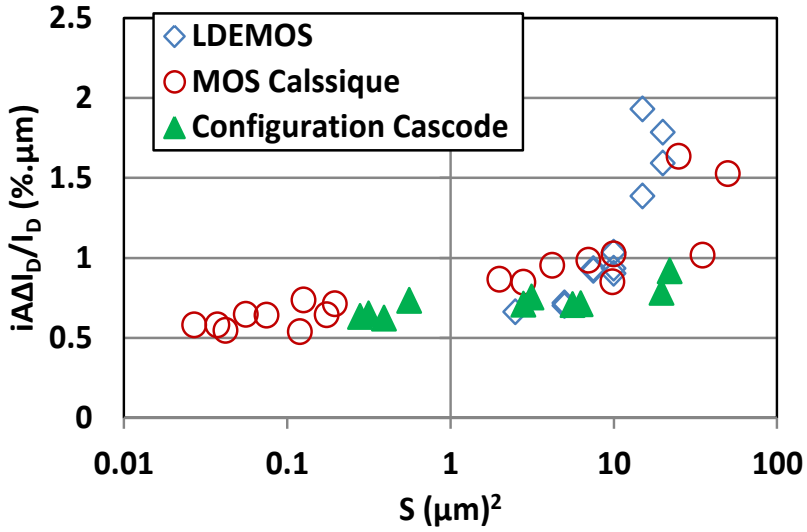

Figure B.9: Comparaison du désappariement de I_D en fonction de la surface des transistors entre le MOSFET classique, le PLDE MOS et la configuration cascode (en régime linéaire)

- En régime linéaire, le nouveau modèle de désappariement de courant de drain de l'Equation B.5 ainsi que le modèle de Croon de l'équation B.4 ont été comparées aux valeurs mesurées pour les trois architectures considérées. Les résultats montrent que le nouveau modèle de désappariement de courant de drain reproduit les mesures pour les trois architectures. Un exemple de cette comparaison est montré dans la Figure B.10 pour le LDEMOS.

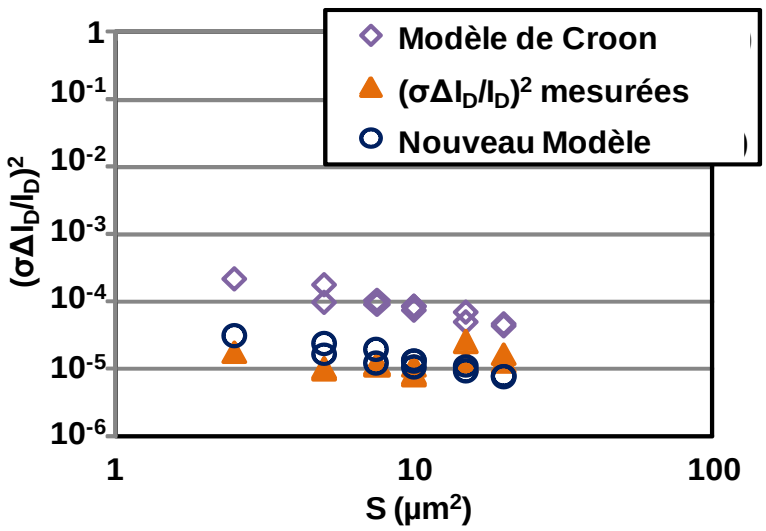

Figure B.10 : Comparaison du désappariement de I_D en fonction de la surface des transistors entre le Modèle de Croon classique, le nouveau modèle proposé dans l'équation 5 et les valeurs mesurés (pour le LDEMOS)

Grâce à une comparaison avec le modèle de Croon, nous avons démontré que la Rsd contribue faiblement à la configuration cascode, et fortement au LDEMOS. Le modèle de l'équation B.5 montre que les comparables valeurs de désappariement des I_D sont dues au Gm/I_D qui présente en valeur absolu des valeurs doubles en MOS individuel classique et cascode configuration par rapport au LDEMOS.

- En régime de saturation, un nouveau modèle de désappariement de courant de drain a été proposé dans l'équation B.6. Ce modèle est basé sur la même approche que celle utilisée en régime linéaire dans le chapitre II et Equation B.5, en partant cette fois de l'équation de courant de drain en régime de saturation. Ce modèle a été appliqué avec succès sur les valeurs mesurées pour le MOS classique individuel, dans la figure B.11, et la configuration cascode. Cependant, ce modèle surestime les valeurs mesurées pour le PLDEMOS. Dans ce cas, le terme $(\frac{Gm}{I_D})^2\sigma^2_{\Delta Vt}$ suffit à reproduire les mesures. Ainsi dans ce régime, le terme $(\frac{Gm}{I_D})$ explique les résultats comparables entre les trois dispositifs de cette étude.

  Dans le futur, plus d'investigations sur la raison de la non reproduction des data par le modèle proposé doivent être menées afin de l'améliorer.

$$\sigma^2_{\Delta I_D/I_D} = (\frac{Gm}{I_D})^2\sigma^2_{\Delta Vt} + \frac{1}{(1+\beta(V_G - Vt)Rsd)}\sigma^2_{\Delta\beta/\beta} \qquad \textbf{(B. 6)}$$

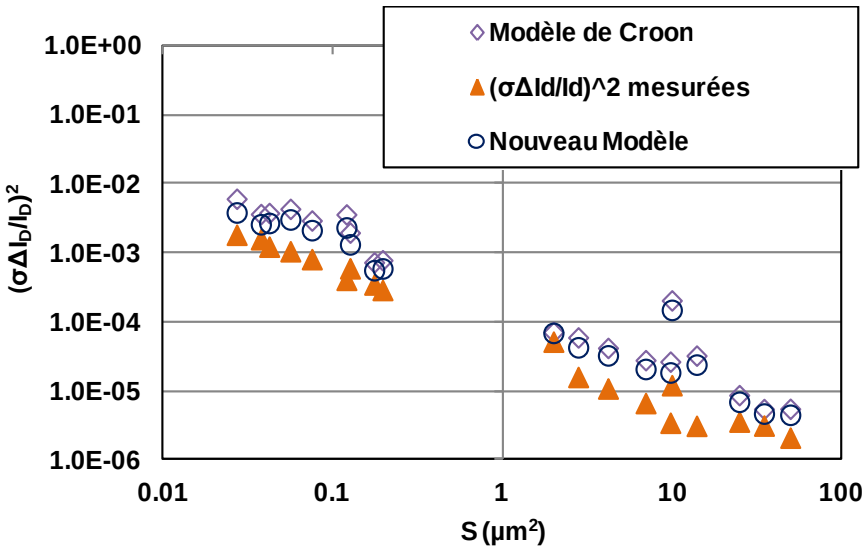

Figure B.11 : Comparaison du désappariement de I_D en fonction de la surface des transistors entre le Modèle de Croon classique, le nouveau modèle proposé dans l'équation 4 et les valeurs mesurées (pour le MOS Individuel classique)

Le travail réalisé dans cette partie de la thèse peut être adapté à des applications spécifiques en fonction des objectifs du designer. Par exemple, considérant que les trois architectures débitent le même courant pour des géométries spécifiques. Une comparaison de la surface de chaque architecture sur silicium ainsi que leurs valeurs de désappariement peuvent être effectués. Une autre approche serait de considérer les mêmes surfaces sur silicium des trois architectures, et dans ce cas des comparaisons de leurs valeurs de courant ainsi que leurs performances désappariement peuvent être réalisées.

Pour le thème d'analyse et modélisation de technologies avancées, les technologies 28 nm Gate-First Bulk et 20nm Gate-Last Bulk, 28nm FD SOI and 14nm FD SOI ont été considérées. Ce thème donne lieu à trois chapitres de la thèse :

- Le chapitre IV propose une étude complète des comportements du désappariement de Vt, β et I_D pour des transistors avec et sans Germanium et avec différents pourcentages de Germanium dans le canal. Cette étude a était réalisée sur des transistors PMOS avec et sans poches de la technologie 28nm Bulk, intégrant du High-k / grille métallique. Les principales conclusions déduites :

  1- Pour des transistors sans poches : ni l'introduction de Ge dans le canal des PMOS ni l'augmentation de son pourcentage (de 20% à 34%) n'ont d'impact significatif sur le désappariement de Vt comme le montre la Figure B.12.

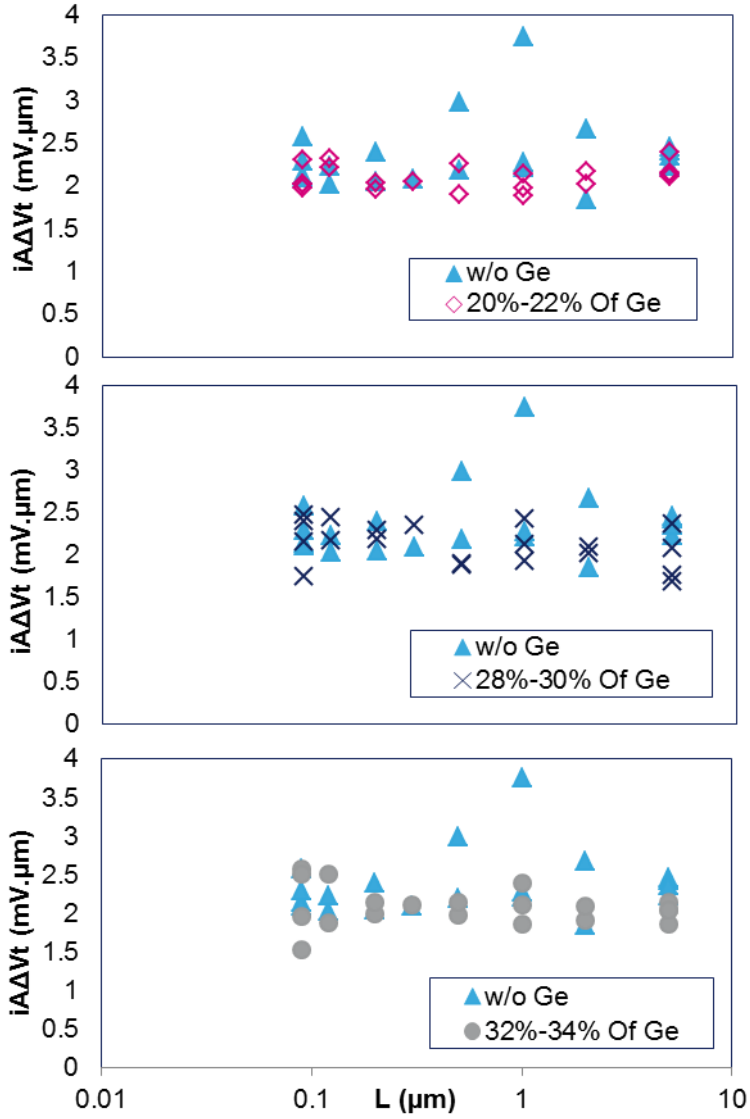

Figure B.12 : Transistors sans poches : Comparaison de $iA_{\Delta Vt}$ en fonction de L entre des transistors sans et avec différents pourcentages de Ge

Ces résultats sont essentiellement dues à :

a- La variabilité négligeable du déplacement de la bande de valence vers le haut comme le montre le Tableau B.2 en utilisant l'équation B.7 :

$$iA_{Ev}(Ge) = \frac{\Delta E_V}{\Delta X} \cdot \frac{\sqrt{X}}{\sqrt{T_{SiGe}.N(Ge)}} \qquad \textbf{(B. 7)}$$

$\frac{\Delta E_V}{\Delta X}$ est la pente de la bande de valence E_V en fonction du pourcentage de Ge X d'après [Soussou 12], i.e. $\frac{\Delta E_V}{\Delta X} = 0.66 eV$, X représente le pourcentage de Germanium, T_{SiGe} représente m'épaisseur de la couche de SiGe et $N(Ge)$ représente la concentration du germanium $(N(Ge) = 4.4 \times 10^{22} at/cm^3)$

Tableau B.2 : iA_{Ev} (%Ge) pour différents pourcentages de Ge utilisant l'Equation B.7

Percentage of Ge	**iA_{Ev} (%Ge) (eV.µm)**
20% - 22% of Ge	1.699×10^{-5} eV.µm
28% - 30% of Ge	2.01×10^{-5} eV.µm
32% - 34% of Ge	2.149×10^{-5} eV.µm

b- La variabilité due à l'épaisseur de la couche de Ge introduite est négligeable. Dans ce cas, une conclusion importante doit être considérée : quand T_{SiGe} (égale 7nm dans notre cas) est assez important (T_{SiGe} >5nm), Vt est stable, et sa variabilité est négligeable. Cependant, quand T_{SiGe} devient très faible (T_{SiGe} >5nm, dans notre cas selon [Soussou12]), cette source de variabilité peut influencer le désappariement de Vt.

2- Pour des transistors avec poches : l'introduction du Ge améliore le désappariement de Vt dans la Figure B.13. En effet lorsque le Ge est introduit, les dopants dans les poches (Arsenic) tendent à diffuser dans le canal. Le contraste entre les dopants des poches et le reste du canal devient moins important améliorant ainsi le désappariement de Vt, pour des longueurs moyennes de canal, comme cela est illustré dans la Figure B.14.

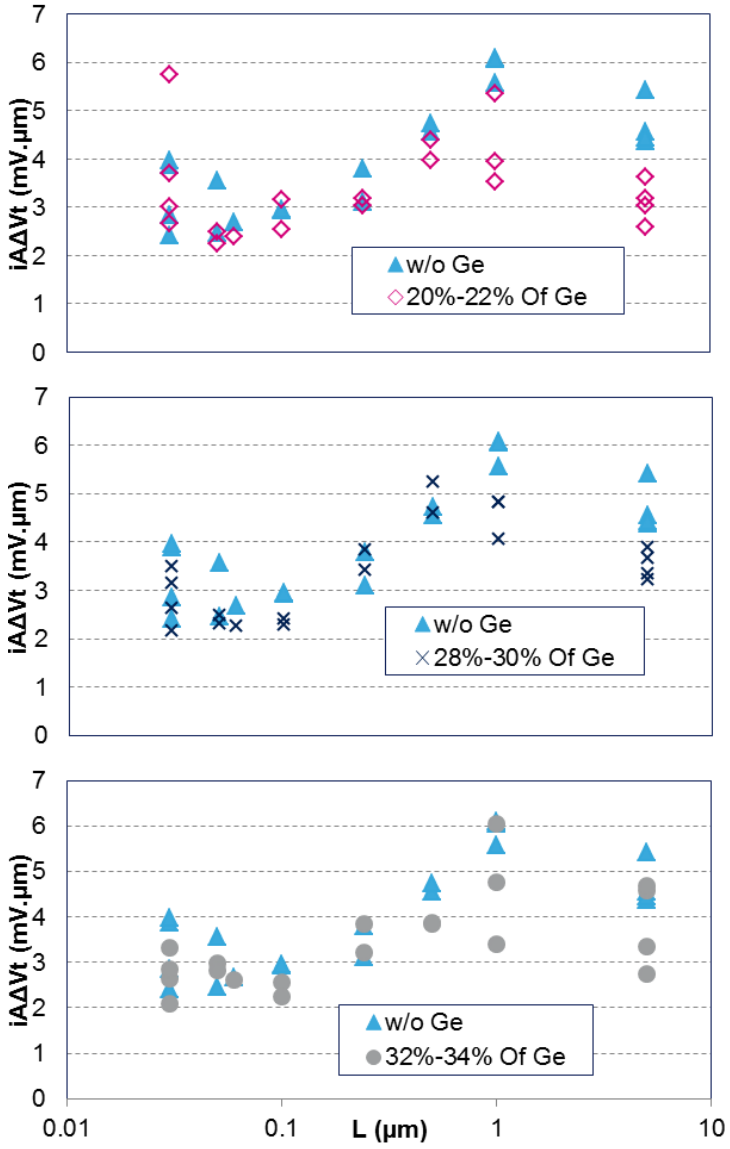

Figure B.13 : Transistors avec Poches : Comparaison de $iA_{\Delta Vt}$ en fonction de L entre des transistors sans et avec différents pourcentages de Ge

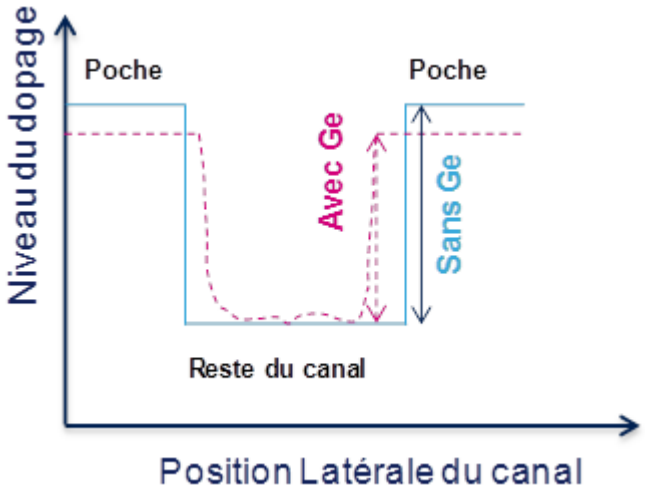

Figure B.14 : Illustration du contraste entre les dopants des poches et le reste du canal pour des transistors avec et sans Ge

3- L'introduction du Ge améliore le désappariement de β pour des transistors avec (Figure B.15) et sans poches. Cela est dû à la réduction du « Coulomb scattering » avec l'introduction du Ge [Diouf 13]. Cependant, l'augmentation du pourcentage de Ge n'induit aucune variation additionnelle du désappariement de β.

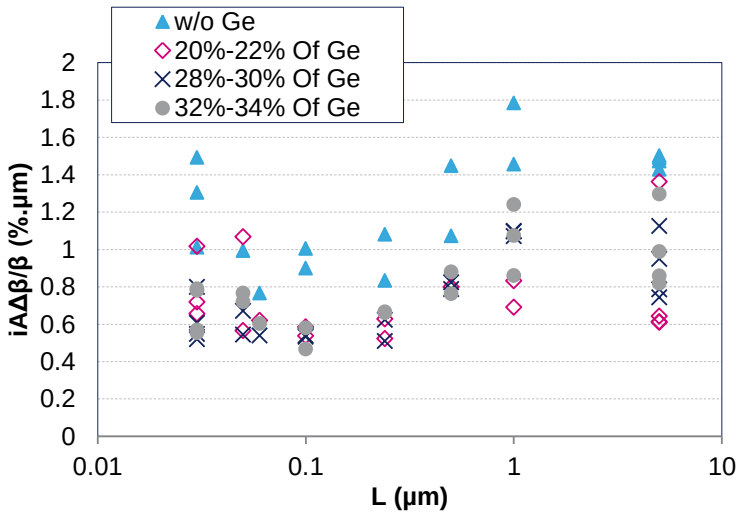

Figure B.15 : Transistors avec Poches : Comparaison de $iA_{\Delta\beta/\beta}$ en fonction de L entre transistors sans et avec différents pourcentages de Ge

4- L'introduction du Ge améliore le désappariement de I_D pour des transistors avec (Figure B.16) et sans poches. Cela est attribué au paramètre Gm/I_D dans le modèle de Croon [Croon 02]. Par contre ce modèle surestime les données mesurées pour

les transistors avec poches. Dans ce cas, plus de paramètres doivent être pris en considération comme la contribution de Rsd étudiée dans le chapitre II de la thèse.

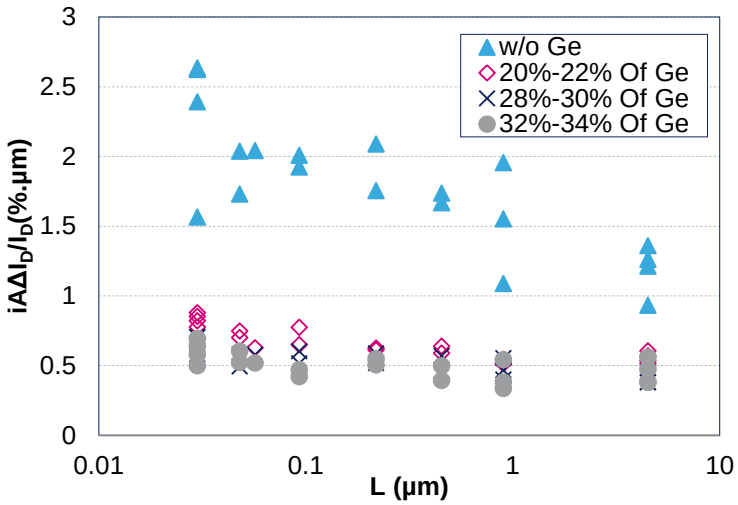

Figure B.16 : Transistors avec Poches : Comparaison de $iA_{\Delta ID/ID}$ en fonction de L entre transistors sans et avec différents pourcentages de Ge

Cette étude fournit une meilleure compréhension des effets de l'introduction du Germanium dans le canal PMOS sur le désappariement de Vt, β et I_D. Elle montre pour la première fois, que l'introduction du Ge peut améliorer, dans certains cas, le désappariement de Vt, β et I_D contrairement à ce qui a était publié dans la littérature. Cette étude décortique les différentes contributions et phénomènes physiques agissant sur le désappariement de Vt, β et I_D avec l'introduction du Ge, et ainsi peut servir comme repère pour les technologies futures qui intègrent du SiGe dans leur canal.

- Le chapitre V traite de l'effet du Métal-Gate-Last sur le désappariement de Vt, β et I_D pour la technologie 20nm Bulk. Les résultats sont ensuite comparés avec le 28 nm Métal-Gate-First Bulk technologie.

  - La comparaison entre les dispositifs GO1 (Tox= 12.48Å/12.7Å (NMOS/PMOS)) et GO2 (Tox= 31.6Å/32.9Å (NMOS/PMOS)) pour la technologie 20nm Métal-Gate-Last montre :

    4. Une meilleure performance des désappariements de Vt et β pour les dispositifs d'oxydes de grille les plus minces (GO1), due à un meilleur

couplage capacitif comme le montre la Figure B.17 (pour le désappariement de Vt).

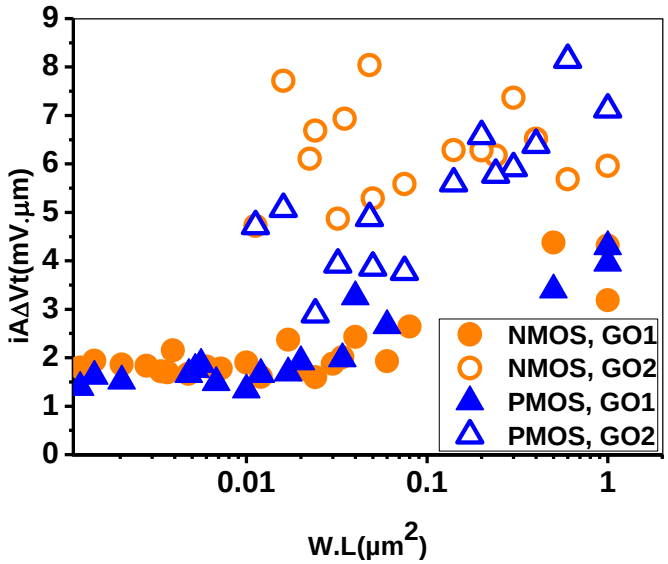

Figure B.17 : Comparaison de $iA_{\Delta Vt}$ (mV.µm) en fonction de la surface des transistors (W.L (µm²)) entre les dispositifs GO1 et GO2 pour les transistors NMOS et PMOS de la technologie 20nm Métal-Gate-Last

5. Des valeurs de $iA_{\Delta Qd}$ identiques entre les oxydes de grille épais (GO2) et mince (GO1) comme le montre la Figure B.18. Cette similarité suggère que le désappariement de Vt est proportionnel à Tox, et que la contribution du canal est dominante par rapport à la contribution de la grille. Ainsi, en introduisant des améliorations dans l'effet de la granularité de la grille métallique (MGG), la technologie Métal-Gate-Last permet la réduction, voire la suppression de la contribution de la grille dans le désappariement de Vt.

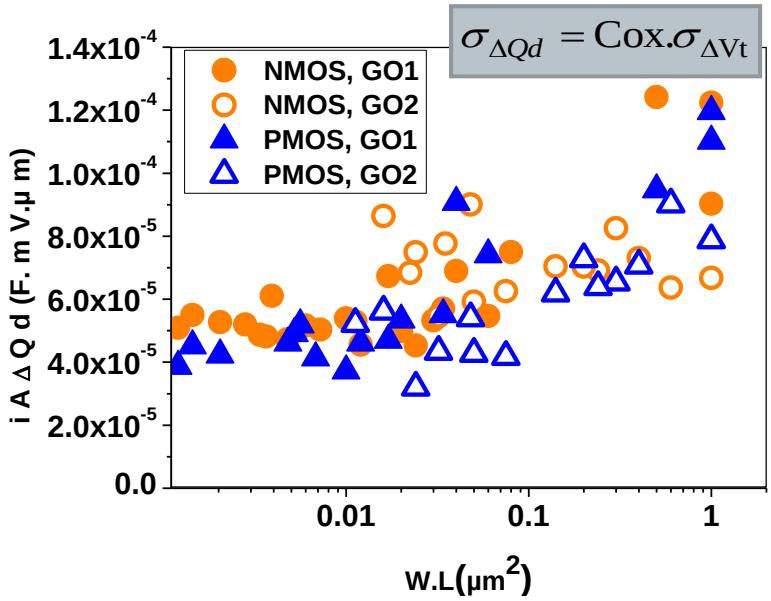

Figure B.18 : Comparaison de $iA_{\Delta Qd}$ (F.mV.µm) en fonction de la surface des transistors (W.L (µm^2)) entre les dispositifs GO1 et GO2, NMOS et PMOS de la technologie 20nm Métal-Gate-Last

6. Des valeurs de désappariement de I_D proches entre les dispositifs GO1 et GO2. Cela est expliqué par la contribution de Rsd et de $|Gm/I_D|$ dans le nouveau modèle de désappariement de I_D proposé dans le chapitre II.

- La comparaison entre les technologies 20nm Métal-Gate-Last et 28 nm Métal-Gate-First montre que la technologie Gate-Last bénéficie d'une amélioration des désappariement de Vt et de β avec des valeurs de $iA_{\Delta Vt}$ très prometteuses comme le montre la Figure B.19.

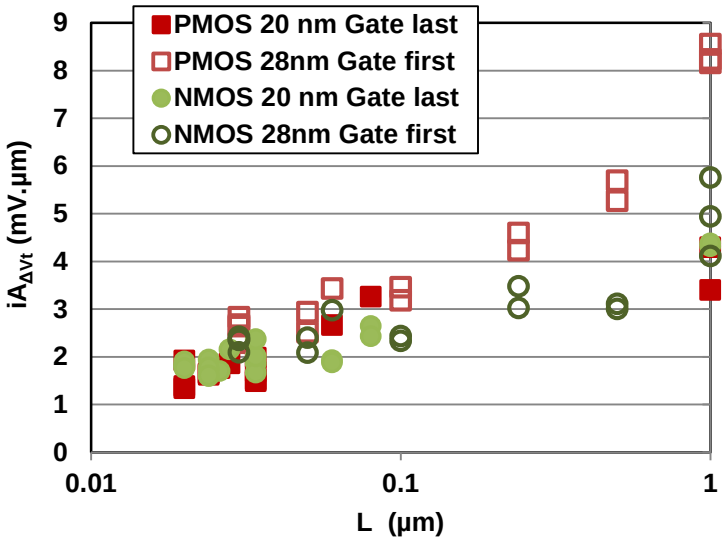

Figure B.19 : Comparaison de iA$_{\Delta Vt}$ (mV.µm) en function de L (µm) entre les technologies 28nm Métal-Gate-First et 20nm Métal-Gate-Last pour les dispositifs NMOS et PMOS

- Le dernier point investigué dans ce chapitre concerne les tendances de désappariement de Vt et β en fonction de Tox en partant de la technologie 90nm de STMicroelectronics jusqu'à la technologie 20nm Gate-Last de IBM. Les résultats montrent que :

    3. iA$_{\Delta Vt}$ est linéaire en fonction de Tox avec un offset plus grand que zéro allant des nœuds technologiques 90nm jusqu'à 45nm. Ces nœuds intègrent une grille poly silicium. Cet offset approche zéro en remplaçant la grille poly par une grille métallique. Ce phénomène est illustré dans la Figure B.20 pour les NMOS. Notons que le même phénomène est aussi observé pour les PMOS

    4. iA$_{\Delta\beta/\beta}$ n'est pas proportionnel à Tox comme le montre la Figure B.21 pour les NMOS. Notons que le même phénomène est aussi observé pour les PMOS.

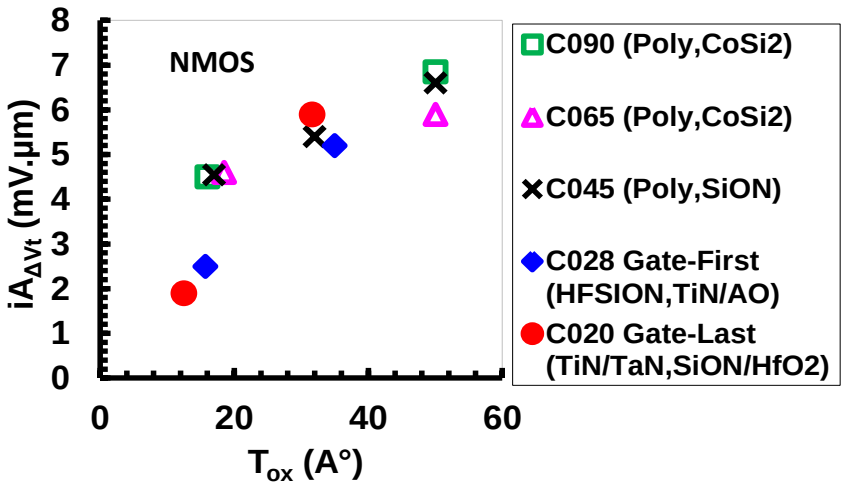

Figure B.20 : Les tendances de $iA_{\Delta Vt}$ (mV.µm) en fonction de l'épaisseur de l'oxyde de la grille Tox (Å) de la technologie 90nm ST Bulk jusqu'à la technologie 20nm Gate-Last Bulk pour des transistors NMOS

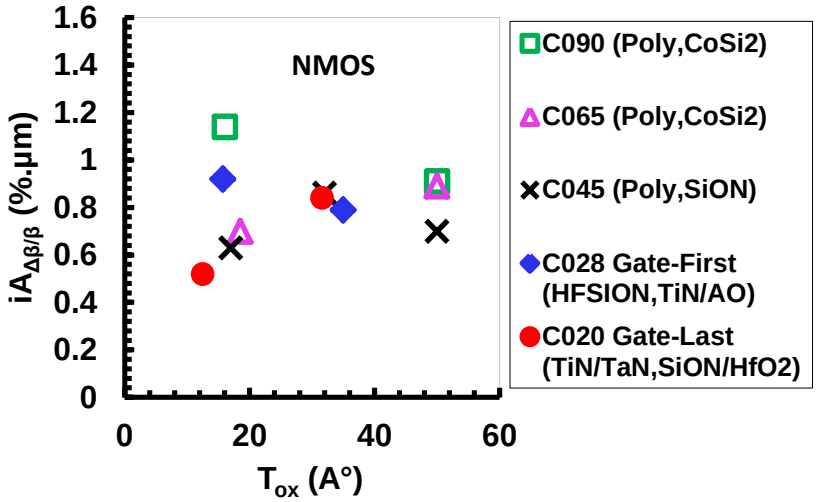

Figure B.21 : Les tendances de $iA_{\Delta\beta/\beta}$ (%.µm) en fonction de l'épaisseur de l'oxyde de la grille Tox (Å) de la technologie 90nm ST Bulk jusqu'à la technologie 20nm Gate-Last Bulk pour des transistors NMOS

Cette étude a confirmé expérimentalement les simulations de Asenov et al.'s dans [Asenov 00], en ce qui concerne l'amélioration du désappariement de Vt en utilisant la grille métallique au lieu du poly-silicium. Elle a montré aussi les avantages de la technologie Gate-Last sur les performances du désappariement. Ainsi elle a investigué le désappariement de β en fonction du Tox pour la première fois dans la littérature. Finalement, elle a confirmé expérimentalement que la principale contribution dans la technologie bulk sur le désappariement de Vt reste le dopage de canal dans les technologies avancés, notamment le 28 et le 20nm.

- Dans la première section du chapitre VI, la technologie 14 nm FD SOI a été étudiée et comparée avec la technologie 28 nm FD SOI.

  - Des performances identiques de désappariement de Vt, β et I_D pour des oxydes de grille mince et épais ont été observées pour les N/P MOS de la technologie 14nm FD SOI dans les figures B.21, B.22 et B.23 respectivement :

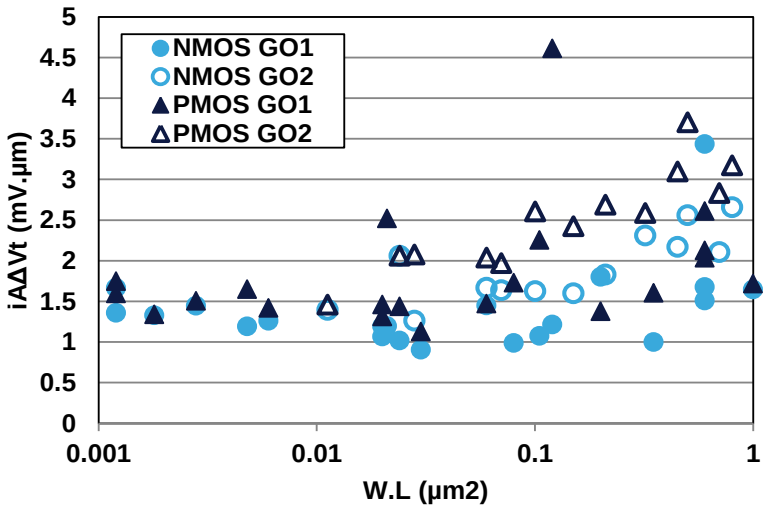

Figure B.21 : Comparaison de $iA_{\Delta Vt}$ (mV.µm) en fonction de la surface des transistors W.L (µm²) entre les GO1 et GO2 pour les dispositifs NMOS et PMOS de la technologie 14nm FD SOI

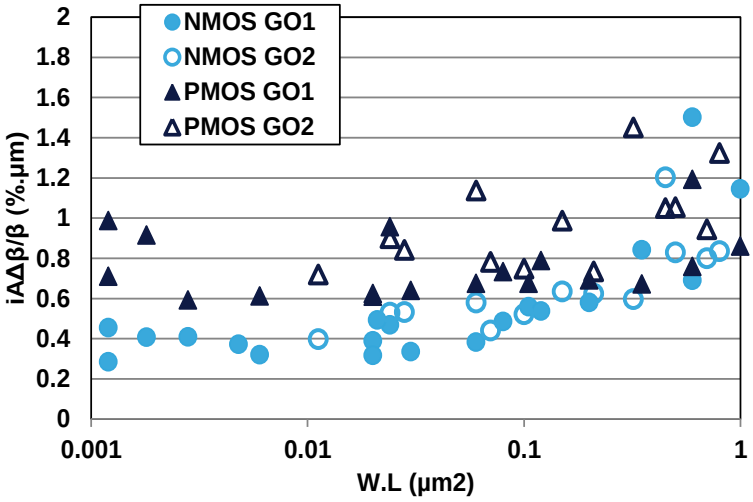

Figure B.22 : Comparaison de $iA_{\Delta\beta/\beta}$ (%.µm) en fonction de la surface des transistors W.L (µm²) entre les GO1 et GO2 pour les dispositifs NMOS et PMOS de la technologie 14nm FD SOI

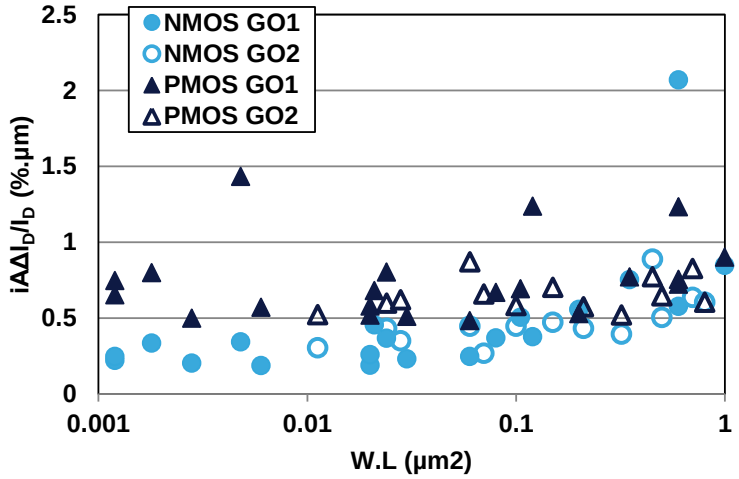

Figure B.23 : Comparaison de $iA_{\Delta ID/ID}$ (%.µm) en fonction de la surface des transistors W.L (µm²) entre les GO1 et GO2 pour les dispositifs NMOS et PMOS de la technologie 14nm FD SOI

- La similarité du désappariement de Vt est attribuée à l'absence des dopants dans le canal dans la technologie FD SOI. Ainsi iAΔVt n'est plus proportionnel à Tox (contrairement à la technologie Bulk), ce qui implique que la contribution de la grille est dominante par rapport à la contribution du canal ;

- Le désappariement de β n'est pas proportionnel à Tox. Ce résultat est similaire à la technologie Bulk du chapitre V ;

- Le nouveau modèle de désappariement de courant de drain, proposé dans le chapitre II a été appliqué avec succès sur les valeurs mesurées. Ainsi, ce modèle explique la similarité entre les dispositifs GO1 et GO2 où le désappariement de I_D est due à la contribution de Rsd, du terme $|Gm/I_D|$ ainsi que des désappariements de Vt et de β.

– En ce qui concerne la technologie 28nm, les résultats montrent que les désappariements de Vt, β et I_D sont à peu près identiques à la technologie 14nm dans les figures B.24, B.25 et B.26. Cela confirme que :

- Le désappariement de Vt est indépendant de Tox, par opposition à ce qui a été observé dans la technologie Bulk.
- Le désappariement de β est aussi indépendant de Tox comme observé pour la technologie Bulk.

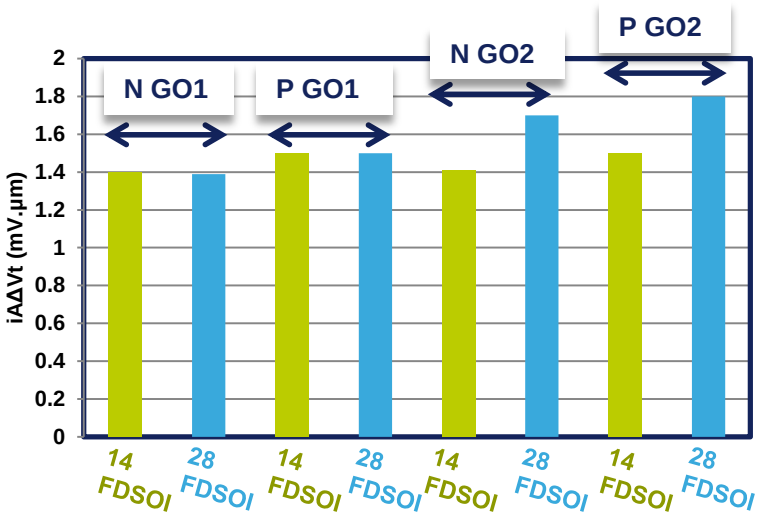

Figure B.24: Les valeurs moyennes de $iA_{\Delta Vt}$ (mV.µm) pour les technologies 28 et 14 nm

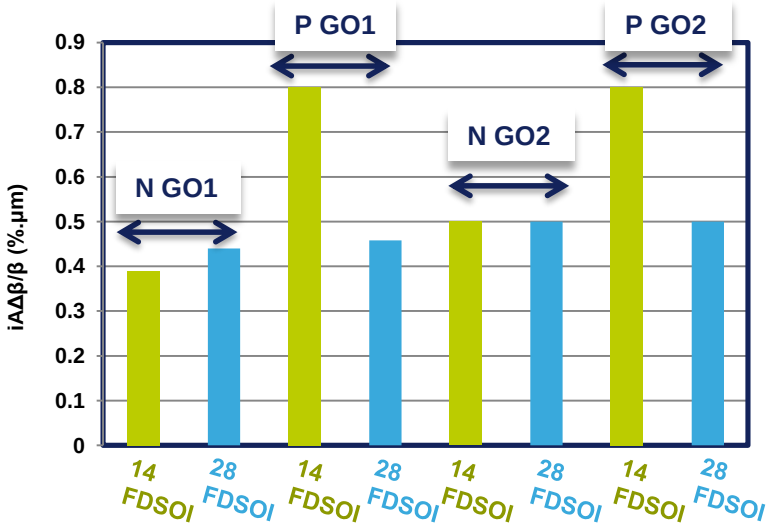

Figure B.25 : Les valeurs moyennes de $iA_{\Delta\beta/\beta}$ (%.µm) pour les technologies 28 et 14 nm

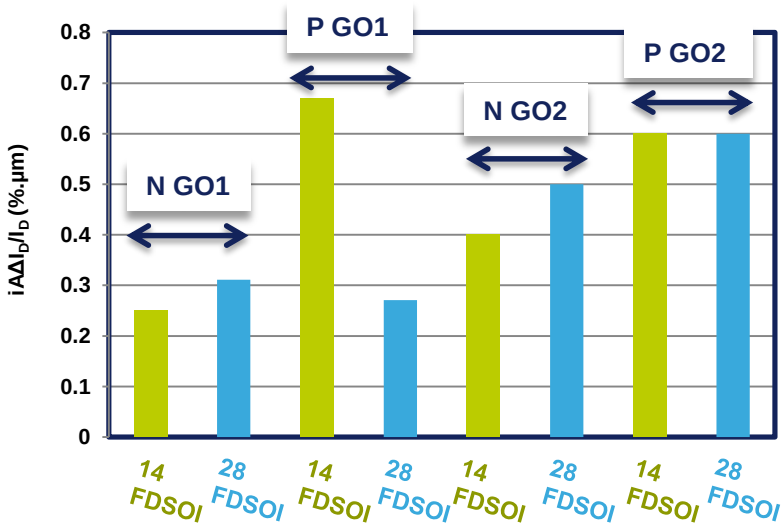

Figure B.26 : Les valeurs moyennes de $iA_{\Delta I_D/I_D}$ (%.µm) pour les technologies 28 et 14 nm

Cette section du chapitre VI a montré que la principale contribution du désappariement de Vt dans les technologies FD SOI avancés est la contribution de la grille. Elle a montré aussi les avantages de l'utilisation de la technologie FD SOI dans les nœuds avancés notamment le 14nm en ce qui concerne les très bonnes performances du désappariement de Vt, β et I_D pour les dispositifs nominaux.

La deuxième section du chapitre VI, traite le dernier thème de la thèse : analyse et modélisation des phénomènes de desappariement des transistors MOS avec leurs vieillissements. La condition de stress Negative Bias Temperature Instability (NBTI), a été utilisée à une température de 125°C pour la technologie 28nm FD SOI. Cette section montre que :

- Le désappariement de Vt est dégradé en fonction des défauts (Nst) (des charges fixes et des états d'interfaces) induits par le NBTI stress à l'interface Si/SiO_2 et dans l'oxyde. Un modèle compact qui dépend directement de Nst a été développé dans l'équation B.8. Ce modèle a été appliqué avec succès sur les valeurs mesurées et explique cette dégradation en fonction du Nst dans la Figure B.27.

$$iA_{\Delta Vt}^2 = iA_{\Delta Vt0}^2 + \frac{q^2 Nst}{Cox^2} \qquad \textbf{(B. 8)}$$

Où $iA^2_{\Delta Vt0}$ est la constante individuelle de désappariement de Vt à 125°C avant le stress

q : la charge égale à $1.6x10^{-19}$ Coulomb

Cox : la Capacité d'oxyde

Ns t : les charges fixes et des états d'interfaces induites par le NBTI stress

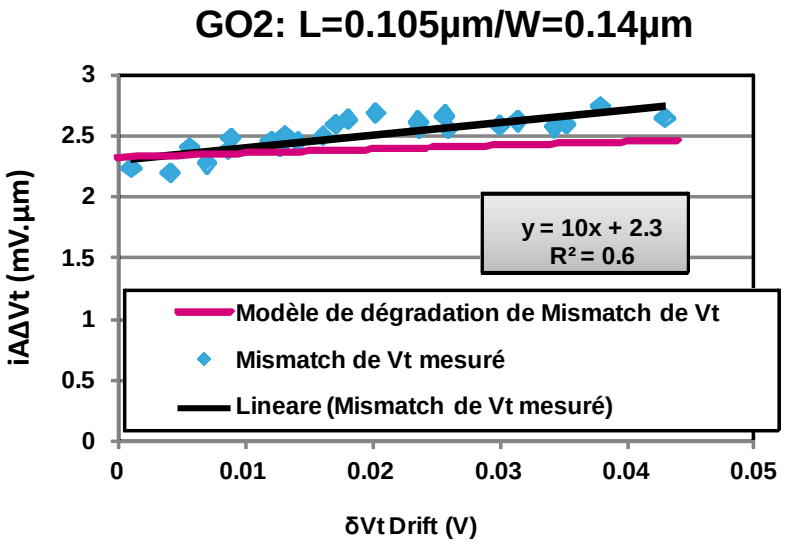

Figure B.27 : L=0.105µm and W=0.14µm : la constant individuelle de désappariement de Vt en fonction du drift de Vt: Comparaison entre les valeurs mesurées et le modèle théorique de l'équation B.8

- Le désappariement de β est faiblement dégradé avec 12% de dégradation dans les pires cas et 1% de dégradation dans les meilleurs cas. Un modèle compact qui dépend directement des valeurs de Nst a également été développé dans l'équation B.9. Cependant ce modèle sous-estime les dégradations réelles des transistors avec le stress NBTI comme le montre la Figure B.28.

$$iA^2_{\Delta\beta/\beta|} = iA^2_{\Delta\beta/\beta|0} + \alpha^2.q^2.Nst.\mu_0^2 \qquad \textbf{(B. 9)}$$

Où $iA^2_{\Delta\beta/\beta|0}$ est la constante individuelle de désappariement de β à 125°C avant le stress.

α : le coefficient de « Remote Coulomb Scattering » exprimée en ($V.s/C^{-1}$)

μ_0 : la mobilité à faible champ

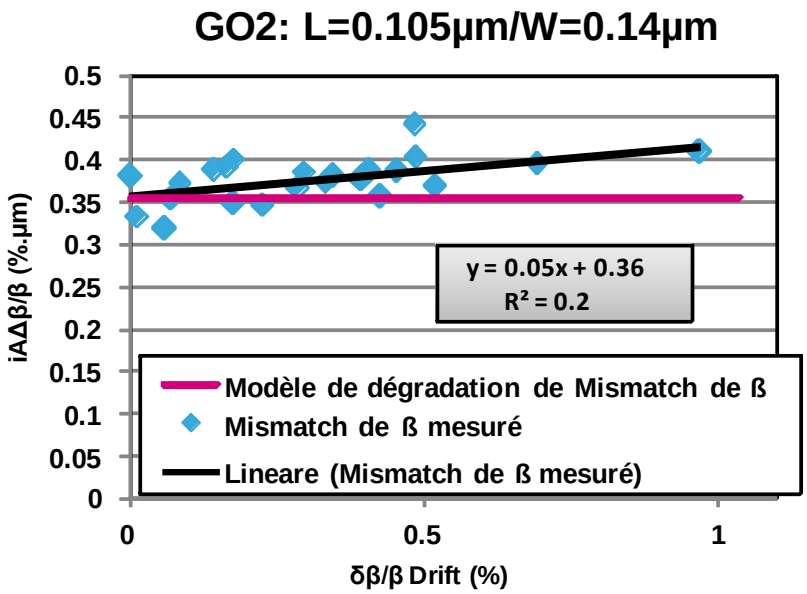

Figure B.28 : L=0.105µm and W=0.14µm : la constant individuelle de désappariement de β en fonction du drift de β: Comparaison entre les valeurs mesurées et le modèle théorique de l'équation B.9

La dernière partie de la thèse a montré un désappariement significatif de Vt et faible de β de la technologie FD SOI en fonction du stress NBTI. Des modèles ont été proposés et peuvent être utilisés pour estimer le niveau de désappariement de Vt et de β en fonction de Nst. Ces modèles peuvent être appliqués et améliorés, dans le futur, sur d'autres technologies comme le 14nm FD SOI et le 28nm Bulk.

Durant cette thèse, 6 articles (Références ci-dessous) ont été présentés dans 4 conférences et deux journaux. Aussi j'ai participé à l'organisation des *"Journées Nationales du Réseau Doctoral en Micro-nanoélectronique (JNRDM 2013)"* d'Octobre 2012 – Juin 2013. Cette conférence a eu lieu à Grenoble du 10 à 12 Juin 2013.

B.IV Articles

Conférences Internationales:

- "Désappariement trends in 20nm Gate-last bulk CMOS technology" **Lama RAHHAL**, Aurelie BAJOLET, Jean-Philippe MANCEAU, Julien ROSA, Stephane RICQ, Sebastien LASSERE, Gerard GHIBAUDO, ULTIMATE INTEGRATION ON SILICON (ULIS), pp.133-136 , Stockholm, Sweden April 2014
- "Cascode configuration as a substitute to LDE MOSFET for improved electrical désappariement performance", **Lama RAHHAL**, Guillaume BERTRAND, Aurelie BAJOLET, Julien ROSA, Gerard GHIBAUDO, 2014 IEEE International Conference on Microelectronic Test Structures (ICMTS), pp. Udine, Italy, March 2014
- "BTI variability Fundamental understandings and Impact on digital logic by the use of extensive dataset" D. Angot, V. Huard, **L. Rahhal**, A. Cros, X. Federspiel, A. Bajolet, Y. Carminati, M. Saliva, E. Pion, F. Cacho, A. Bravaix, 2013 IEEE **International Electron Devices Meeting** (IEDM), pp. 15.4.1-15.4.4, 2013
- "New methodology for drain current local variability characterization using Y function method", **L. RAHHAL**, A. BAJOLET, C.DIOUF, A.CROS, J.ROSA, N.PLANES, G.GHIBAUDO, 2013 IEEE International Conference on Microelectronic Test Structures (ICMTS), pp 99 -103, Osaka, Japan, March 2013

Papiers Journaux :

- "A comparative désappariement study of the 20nm Gate-last and 28nm Gate-first bulk CMOS technologies" **Lama RAHHAL**, Aurelie BAJOLET, Jean-Philippe MANCEAU, Julien ROSA, Stephane RICQ, Sebastien LASSERE, Gerard GHIBAUDO, Solid State Electronics V. pp., 2014
- "Impact of Ge proportion on advanced SiGe bulk P-MOSFET matching performances", **Lama Rahhal**, Aurélie Bajolet, Antoine Cros, Cheikh Diouf, Flore Kergomard, Julien Rosa, Gregory Bidal, Raul-Andres Bianchi, Gérard Ghibaudo, Solid State Electronics V.85 pp 15-22, 2013

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Résumé:

Afin de réaliser correctement leur fonction, certains blocs analogiques ou numériques comme les miroirs de courant ou les SRAM, nécessitent des paires de transistors MOS électriquement identiques. Cependant, les dispositifs sur silicium, même appariés, subissent des variations locales aléatoires ce qui fait varier leurs performances électriques. Ce phénomène est connu sous le nom désappariement. L'objectif de cette thèse est de comprendre les causes physiques de ce désappariement, de le quantifier et de proposer des solutions pour le réduire. Dans ce contexte, quatre thèmes principaux sont développés. Le premier thème se focalise sur l'optimisation des méthodologies de mesures des phénomènes de désappariement. Une nouvelle méthode de mesure du désappariement de Vt et de β ainsi qu'un nouveau modèle de désappariement de I_D sont proposés, analysés et appliqués à des données mesurées sur des technologies 28nm Bulk et FD SOI. Le second thème se concentre sur la caractérisation des différentes configurations de transistor MOS afin de proposer l'architecture optimale en fonction des applications visées. Ainsi, la possibilité de remplacer le LDEMOS par une configuration cascode est analysée en détail. Le troisième thème se focalise sur l'analyse et la modélisation des phénomènes de désappariement des transistors MOS avancés. Trois aspects sont analysés : 1) l'introduction du Ge dans le canal P des technologies 28nm BULK, 2) la suppression de la contribution de la grille sur le désappariement de Vt en utilisant la technologie 20 nm métal-Gate-Last 3) un descriptif des principaux contributeurs au désappariement de Vt, β et I_D dans les technologies 28 et 14nm FD SOI. Le dernier thème traite du comportement du désappariement des transistors MOS après vieillissement. Un vieillissement NBTI a été appliqué sur des PMOS de la technologie 28nm FD SOI. Des modèles de comportement de Vt et de β en fonction du nombre de charges fixes ou d'états d'interfaces induits à l'interface Si/SiO_2 ou dans l'oxyde sont proposés et analysés.

Mots Clés : Désappariement, transistors MOS, Vt, β, I_D, 28nm Bulk, LDEMOS, configuration cascode, 20nm Métal-Gate-Last, 28nm FD SOI, 14nm FDSOI, NBTI.

Abstract:

For correct operation, certain analog and digital circuits, such as current mirrors or SRAM, require pairs of MOS transistors that are electrically identical. Real devices, however, suffer from random local variations in the electrical parameters, a problem referred to as mismatch. The aim of this thesis is to understand the physical causes of mismatch, to quantify this phenomenon, and to propose solutions that enable to reduce its effects. In this context, four major areas are treated. The first one focuses on the optimization of mismatch measurement methodologies. A new technique for the measurement of Vt and β mismatch and an I_D mismatch model are proposed, analyzed and applied to experimental data for 28 nm Bulk and FD SOI technologies. The second area focuses on the characterization of different configurations of MOS transistors in order to propose design architectures that are optimized for certain applications. Specifically, the possibility of replacing LDEMOS with transistors in cascode configuration is analyzed. The third area focuses on the analysis and modeling of mismatch phenomena in advanced Bulk and SOI transistors. Three aspects are analyzed: 1) the impact of the introduction of germanium in P channel of 28nm BULK transistors; 2) the elimination of the metal gate contribution to Vt mismatch by using 20nm Gate-last Bulk technology; 3) a descriptive study of the principal contributions to Vt, β and I_D mismatch in 28 and 14 nm FD SOI technologies. The last area treats the mismatch trends with transistor aging. NBTI stress tests were applied to PMOS 28nm FD SOI transistors. Models of the Vt and β mismatch trends as a function of the induced interface traps and fixed charges at the Si/SiO_2 interface and in the oxide were developed and discussed.

Key words: Mismatch, transistors MOS, Vt, β, I_D, 28nm Bulk, 20nm Metal-Gate-Last, LDEMOS, cascode configuration, 28nm FD SOI, 14nm FDSOI, NBTI.